1. Overview

The Vortex86DX3 is a 32-bit x86-architecture dual-core microprocessor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 64-Kbyte 8-way L1 cache, 512-Kbyte write through/write back 4-way L2 cache, PCIe bus, DDR3, ROM controller, ISA, I2C, SPI, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet, FIFO UART, USB2.0 Host and IDE/SATA controller within a single 720-pin BGA package system-on-a-chip (SOC). It provides an ideal solution for the embedded system and communications products (such as PC/104, SMARC, thin client, NAT router, home gateway, access point ..etc) to bring about desired performance.

2. Features

- **Dual Processor Core**
  - 1000 MHz (maximum)
  - Symetric multi-processors
  - 6-stage pipeline
  - X86 instruction set
- **Floating Point Unit Support**
  - Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture
- **Branch Prediction Unit**
  - Branch target buffer
- **Translation Lookaside Buffer**
  - 4-Kbyte page I-TLB 64 entries/ 4-Kbyte page D-TLB 64 entries
  - 4-Mbyte page I-TLB 8 entries/ 4-Mbyte page D-TLB 8 entries
- **Embedded I / D Separated L1 Cache**
  - 8-way 32-Kbyte I-Cache, 8-way 32-Kbyte write through D-Cache
- **Embedded Unified L2 Cache**
  - 4-way 512-Kbyte L2 Cache
  - Write through or write back policy
- **DDR3 Control Interface**
  - 32-bit data bus
  - DDR3 size up to 2 Gbytes
- **GPU Control Unit**
  - UMA Architecture
  - VGA Controller
  - 2D Graphics Engine support
  - Supports Single Display max resolution up to 1920x1440@60Hz
  - Supports Dual Display max resolution up to 1280X1024@60Hz
  - Supports Display Device with one D-sub Analog Interface
  - Supports Display Device with one 24-bit or two 12-bit DVO Digital Interface to connect a third party LVDS/TMDS transmitter
  - Supports Display Device for TTL Panel with one 24-bit DVO Digital Interface
  - Support two DSP to accelerate Video decode for MPEG2 MP@HL, VC-1

AP@L2 720P up to 20Mbps, and H.264 HP@L4.1 1080P up to 40Mbps video decode. (Opitional)

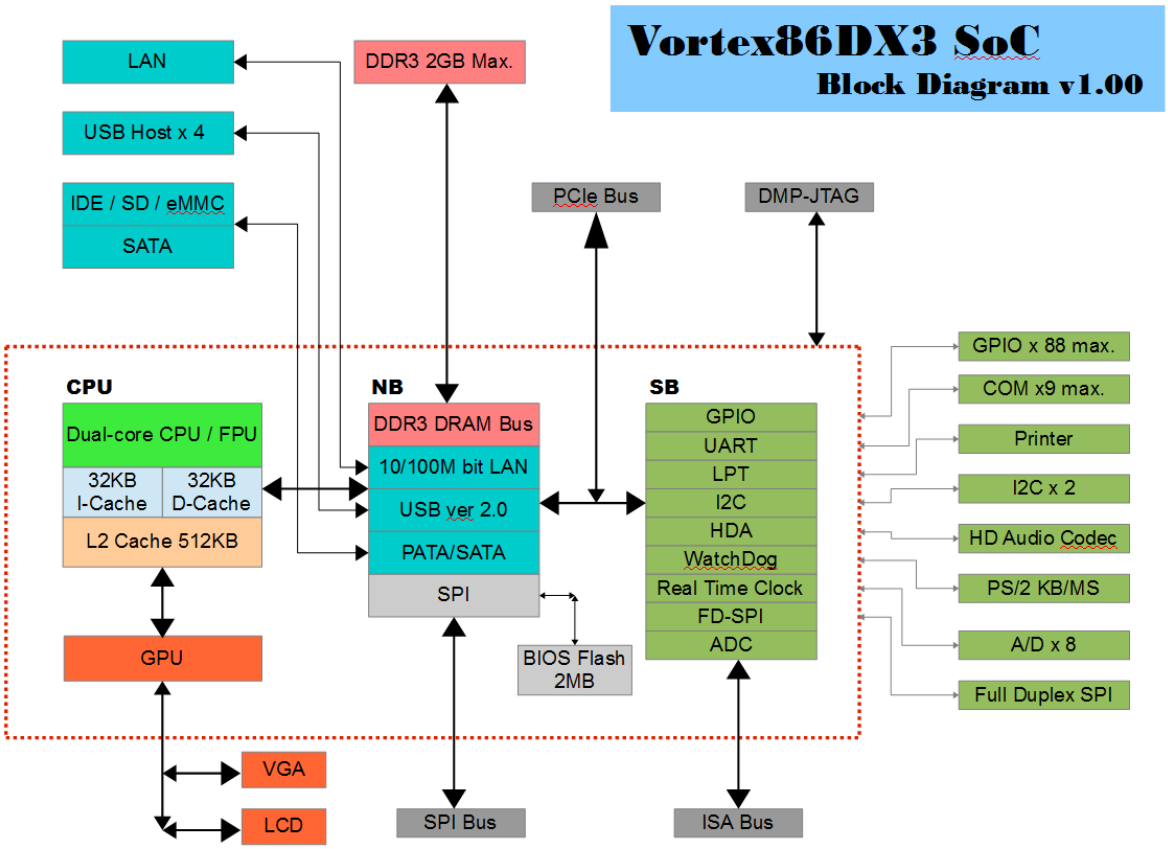
- **DSP Control Unit** (Opitional)
  - 6-stage pipeline
  - 64-Kbyte I-Local SRAM, 4-Kbyte D-Local SRAM
  - 4-way 4-Kbyte I-Cache, 4-way 16-Kbyte D-Cache
- **Fast Ethernet Controller**
- **Internal embedded 2-Mbyte Flash**
  - For BIOS storage
- **SPI Interface x1**
  - For boot up function from SPI flash
- **DMP JTAG Interface supported for software debugging**
- **IDE Controller**
  - PATA 100 (HDD x 2) or SD x 2 at Primary Channel
  - SATA 1.5Gb/s (1 Port) at Secondary Channel
- **PCIe Control Interface x 2**
  - Up to 2 sets of PCIe device
  - 3.3V I/O
- **USB 2.0 Host Support**
  - 4 ports
  - Supports HS, FS and LS
- **HDA Controller**
- **ISA Bus Interface**
  - AT clock programmable
  - 8/16 Bit ISA device with Zero-Wait-State
  - Generate refresh signals to ISA interface during DRAM refresh cycle
  - Supports Max ISA Clock up to 33M
- **DMA Controller**
- **8259 Interrupt Controller**
- **Counter / Timers**
  - 2 sets of 8254 timer controllers (one for system, the other used as PWM Timer)
  - Output on the 2nd PWM Timer Controller
- **WatchDog x 2 sets**
  - From 30.5μ sec. to 512 sec.
- **Read Time Clock**
  - Less than 2.5uA (3.0V) power consumption in Internal RTC Mode while chip is power-off
- **PS/2 Keyboard & Mouse Controller**
  - Compatible with 8042 controller
- **FIFO UART Port x 9 (9 sets of COM Port)**
  - Compatible with 16C550 / 16C552
  - Default internal pull-up
  - Supports the programmable baud rate generator with the data rate from 50 to 3Mbps
  - The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
  - Supports TXD_EN Signal on COM1/2/3/4
  - Port 80h output data could be sent to COM1 by software programming
- **Parallel Port**
  - Supports SPP/EPP/ECP mode
- **Speaker out**
- **General Programmable I/O**

- Supports 88 programmable I / O pins
- Each GPIO pin can be individually configured to be an input/output pin
- GPIO_P0 and GPIO_P1 with interrupt support (input/output)

- **Redundant System Support**
- **I²C bus x 2**
  - Compliant with V2.1
  - Does not support master code of general call, START and CBUS.
- **MTBF Counter**
- **11-bit ADC x 8 channels**
  - Effective Number of Bit=10 bits
- **Motion Control Interface** (Opitional)
  - 3 groups of controller, 4 controllers per group
  - Each controller can configure to PWM/Servo/Sensor Interface mode
  - Controller interconnect to the other with routing network in the same group
  - 8051 Internal Motion Control Support
- **General Shift Interface Support**
  - 2 channels
- **Full Duplex SPI bus x 2**
- **Input Clock**
  - 25 MHz
  - 14.318MHz
  - 32.768KHz
- **Operating Voltage Range**
  - Core Voltage: 1.0V± 5%
  - I/O Voltage: 1.2V ± 5%, 1.5V ± 5%, 1.8V ± 5%, 3.3 V ± 10 %
- **Operating Temperature**
  - -40℃ ~ +85℃
- **Package Type**
  - 31x31mm, 720 Ball PBGA

3. Block Diagram & PCI Device List

3.1. VORTEX86DX3 Block Diagram



3.2. PCI Device List

ID SEL	AD 11	AD 12	AD 13	AD 14	AD 15	AD 16	AD 17	AD 18	AD 19	AD 20	AD 21	AD 22	AD 23	AD 24	AD 25	AD 26	AD 27
Device#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Function	NB	PCIe0	PCIe1					SB	MAC		USB 2.0 HOST		IDE	VGA	HDA	USB Device	
Fun0	NB0							SB0			OHCI						MC
Fun1	NB1							SB1			EHCI						8051 B
Fun2																	SPI0
Fun3																	SPI1

Note:

1. USB 2.0 Host Controller supports 4 ports
2. PCIe0, PCIe1 Interrupt Routing: INTA, INTB, INTC, INTD

4. Terminology Explanation

4.1. Input & Output and Register AttributeTerms

Term	Term Description
I	Input Pin.
O	Output Pin.
I/O	Bi-directional Input/Output Pin.
P	Power Pin.
G	Ground Pin.
RO	Read Only.
WO	Write Only.
R/W	Read and Write.
R/W1C	Read and Write Clear. A register bit with this attribute can be read and written. However, a write of 1 clears the corresponding bit and a write of 0 will have no effect.
W1C	A write of 1 clears this bit.
RC	Read Clear.

5. PIN Function List

5.1. Pin List Table

Function	Symbol	PIN Sum
SYSTEM	PWRGOOD, CLK25MOUT, CLK24MOUT, XOUT_14318, XIN_14318, SPEAKER, PCIRST#	7 PINs
Internal Connection	I_XIN_25M, G_XIN_14318	2 PINs
DDR3 Interface	DRAMRST#, DRAMCLK, DRAMCLK1, DRAMCLK#, DRAMCLK#1, RAS#, CAS#, WE#, CKE, CKE1, CS0#, CS1#, DQM[3:0], DQS[3:0], DQS#[3:0], ODT[0], ODT[1], ZQ, BA[2:0], MD[31:0], MA[15:0].	78 PINs
USB Interface	USB_DP,USB_DM, USB1_DP, USB1_DM, USB2_DP, USB2_DM, USB3_DP, USB3_DM USB_REXT, USB_REXT1, USB_REXT2, USB_REXT3	12 PINs
ISA Bus Interface	IOCHCK#, IOCHRDY, AEN, 0WS#, MEMR#, MEMW#, SMEMR#, SMEMW#, IOW#, IOR#, REFRESH#, SYSCLK, TC, BALE, SBHE#, MEMCS16#, IOCS16#, OSC14318, RST_DRV, IRQ[15:14], IRQ[12:9], IRQ[7:3], DRQ[7:5], DRQ[3:0], DACK#[7:5], DACK#[3:0], SD[15:0], SA[19:0], LA[23:17]	87 PINs
Chip Selection	GPCS0# / STRAP_PLL, GPCS1# / STRAP_PLL1_SEL	2 PINs
SPI Interface	SPI_CS# / ROM_CS# / STRAP_BMS, SPI_CK / STRAP_JTAG, SPI_DO / STRAP_FLASH_SEL, SPI_DI	4 PINs
Redundant	EXTSYSFAILIN#, SYSFAILOUT#, EXT_SWITCH_FAIL#, EXT_GPCS#	4 PINs
KBD / MOUSE Interface	KBCLK/KBRST#, KBDAT/A20GATE#, MSCLK, MSDAT	4 PINs
RTC Interface	RTC_PS, RTC_XOUT, RTC_XI	3 PINs
PCIe Bus Interface	PE_RXP, PE_RXN, PE_TXP, PE_TXN, PE1_RXP, PE1_RXN, PE1_TXP, PE1_TXN, PE_CLKP, PE_CLKN, DIF_PE_PLLCLK100_P, DIF_PE_PLLCLK100_N, DIF_PE_CLK100_P, DIF_PE_CLK100_N, DIF1_PE_CLK100_P, DIF1_PE_CLK100_N	16 PINs

Function	Symbol	PIN Sum
INTERNAL SPI CONTROL	SPIFL_WP#, SPIFL_Hold#	2 PINs
JTAG Interface	TDO, TMS, TCK, TDI	4 PINs
COM5 / GPIO_P0[7:0] / 8051A_P0[7:0] / MC3[1:0],MC0[4,5,3:0] / 8051B_P0[7:0] / 8051B[SOUT1,SIN1,TXD_EN1,TXD_EN2], FD_SPI2	CTS5# / GPIO_P0[7] / 8051A_GPIO_P0[7] / MC3[1] / 8051B_GPIO_P0[7] / 8051B_SOUT1, DSR5# / GPIO_P0[6] / 8051A_GPIO_P0[6] / MC3[0] / 8051B_GPIO_P0[6] / 8051B_SIN1, DTR5# / GPIO_P0[5] / 8051A_GPIO_P0[5] / MC0[4] / 8051B_GPIO_P0[5] / 8051B_TXDEN1, SIN5 / GPIO_P0[4] / 8051A_GPIO_P0[4] / MC0[5] / 8051B_GPIO_P0[4] / 8051B_TXDEN2, RI5# / GPIO_P0[3] / 8051A_GPIO_P0[3] / MC0[3] / 8051B_GPIO_P0[3] / FD_SPI2_DI, RTS5# / GPIO_P0[2] / 8051A_GPIO_P0[2] / MC0[2] / 8051B_GPIO_P0[2] / FD_SPI2_DO, SOUT5 / GPIO_P0[1] / 8051A_GPIO_P0[1] / MC0[1] / 8051B_GPIO_P0[1] / FD_SPI2_CLK, DCD5# / GPIO_P0[0] / 8051A_GPIO_P0[0] / MC0[0] / 8051B_GPIO_P0[0] / FD_SPI2_CS#	8 PINs
COM6 / GPIO_P1[7:0] / 8051A_P1[7:0] / MC3[3:2],MC1[4,5,3:0] / 8051B_P1[7:0]	CTS6# / GPIO_P1[7] / 8051A_GPIO_P1[7] / MC3[3] / 8051B_GPIO_P1[7], DSR6# / GPIO_P1[6] / 8051A_GPIO_P1[6] / MC3[2] / 8051B_GPIO_P1[6], DTR6# / GPIO_P1[5] / 8051A_GPIO_P1[5] / MC1[4] / 8051B_GPIO_P1[5], SIN6 / GPIO_P1[4] / 8051A_GPIO_P1[4] / MC1[5] / 8051B_GPIO_P1[4], RI6# / GPIO_P1[3] / 8051A_GPIO_P1[3] / MC1[3] / 8051B_GPIO_P1[3], RTS6# / GPIO_P1[2] / 8051A_GPIO_P1[2] / MC1[2] / 8051B_GPIO_P1[2], SOUT6 / GPIO_P1[1] / 8051A_GPIO_P1[1] / MC1[1] / 8051B_GPIO_P1[1], DCD6# / GPIO_P1[0] / 8051A_GPIO_P1[0] / MC1[0] / 8051B_GPIO_P1[0],	8 PINs

Function	Symbol	PIN Sum
COM7 / GPIO_P2[7:0] / 8051A_P2[7:0] / MC3[5:4],MC2[4,5,3:0] / 8051B_P2[7:0] / SA[31:24]	CTS7# / GPIO_P2[7] / 8051A_GPIO_P2[7] / MC3[5] / 8051B_GPIO_P2[7] / ISA_SA[31], DSR7# / GPIO_P2[6] / 8051A_GPIO_P2[6] / MC3[4] / 8051B_GPIO_P2[6] / ISA_SA[30], DTR7# / GPIO_P2[5] / 8051A_GPIO_P2[5] / MC2[4] / 8051B_GPIO_P2[5] / ISA_SA[29], SIN7 / GPIO_P2[4] / 8051A_GPIO_P2[4] / MC2[5] / 8051B_GPIO_P2[4] / ISA_SA[28], RI7# / GPIO_P2[3] / 8051A_GPIO_P2[3] / MC2[3] / 8051B_GPIO_P2[3] / ISA_SA[27], RTS7# / GPIO_P2[2] / 8051A_GPIO_P2[2] / MC2[2] / 8051B_GPIO_P2[2] / ISA_SA[26], SOUT7 / GPIO_P2[1] / 8051A_GPIO_P2[1] / MC2[1] / 8051B_GPIO_P2[1] / ISA_SA[25], DCD7# / GPIO_P2[0] / 8051A_GPIO_P2[0] / MC2[0] / 8051B_GPIO_P2[0] / ISA_SA[24],	8 PINs
Ext RTC / GPIO_P3[7-4] / 8051A_P3[7:4] / TX_DEN[4:3], 8051B_P3[5:4] / COM8[CTS,DSR,DTR,SIN] / I^2C1, I^2C	RTC_AS/GPIO_P3[7]/8051A_GPIO_P3[7]/COM4_TXDEN/CTS8#/I2C1_SDA, RTC_RD# / GPIO_P3[6] / 8051A_GPIO_P3[6] / COM3_TXDEN / DSR8# / I2C1_SCL, RTC_WR# / GPIO_P3[5] / 8051A_GPIO_P3[5] / 8051B_SOUT2 / 8051B_GPIO_P3[5] / DTR8#/I2C_SDA, RTC_IRQ8# / GPIO_P3[4] / 8051A_GPIO_P3[4] / 8051B_SIN2 / 8051B_GPIO_P3[4] / SIN8/I2C_SCL	4 PINs
External SPI / GPIO_P3[3-0] / 8051A_P3[3:0] / FD_SPI1 / 8051B_GPIO_P3[3] / COM8[RI,RTS,SOUT,DCD]	E_SPI_DI / GPIO_P3[3] / 8051A_GPIO_P3[3] / FD_SPI1_DI / 8051B_GPIO_P3[3] / RI8#, E_SPI_DO / GPIO_P3[2] / 8051A_GPIO_P3[2] / FD_SPI1_DO / 8051B_GPIO_P3[2] / RTS8#, E_SPI_CLK / GPIO_P3[1] / 8051A_GPIO_P3[1] / FD_SPI1_CLK / 8051B_GPIO_P3[1] / SOUT8 / 8051B_SOUT2, E_SPI_CS# / GPIO_P3[0] / 8051A_GPIO_P3[0] / FD_SPI1_CS# / 8051B_GPIO_P3[0] / DCD8#	4 PINs
COM1 / GPIO_P4[7:0]	CTS1# / GPIO_P4[7] / 8051A_GPIO_P4[7] / MC7[1] /	8 PINs

Function	Symbol	PIN Sum
/ 8051A_GPIO_P4[7:0] / MC7[1:0],MC4[4,5,3:0] / 8051B_GPIO_P4[7:0]	8051B_GPIO_P4[7], DSR1# / GPIO_P4[6] / 8051A_GPIO_P4[6] / MC7[0] / 8051B_GPIO_P4[6], DTR1# / GPIO_P4[5] / 8051A_GPIO_P4[5] / MC4[4] / 8051B_GPIO_P4[5], SIN1/GPIO_P4[4] / 8051A_GPIO_P4[4] / MC4[5] / 8051B_GPIO_P4[4], RI1#/GPIO_P4[3] / 8051A_GPIO_P4[3] / MC4[3] / 8051B_GPIO_P4[3], RTS1# / GPIO_P4[2] / 8051A_GPIO_P4[2] / MC4[2] / 8051B_GPIO_P4[2], SOUT1 / GPIO_P4[1] / 8051A_GPIO_P4[1] / MC4[1] / 8051B_GPIO_P4[1], DCD1# / GPIO_P4[0] / 8051A_GPIO_P4[0] / MC4[0] / 8051B_GPIO_P4[0]	
PWM / GPIO_P5[7:0] / MC7[3:2],MC5[4,5,3:0] / 8051B_GPIO_P5[7:0] / COM2	PWM1_GATE / GPIO_P5[7] / MC7[3] / 8051B_GPIO_P5[7] / CTS2#, PWM_GATE / GPIO_P5[6] / MC7[2] / 8051B_GPIO_P5[6] / DSR2#, PWM2_OUT / GPIO_P5[5] / MC5[4] / 8051B_GPIO_P5[5] / DTR2#, PWM2_CLK / GPIO_P5[4] / MC5[5] / 8051B_GPIO_P5[4] / SIN2, PWM1_CLK / GPIO_P5[3] / MC5[3] / 8051B_GPIO_P5[3] / RI2#, PWM1_OUT / GPIO_P5[2] / MC5[2] / 8051B_GPIO_P5[2] / RTS2#, PWM_OUT / GPIO_P5[1] / MC5[1] / 8051B_GPIO_P5[1] / SOUT2, PWM_CLK / GPIO_P5[0] / MC5[0] / 8051B_GPIO_P5[0] / DCD2#	8 PINs
Primary IDE Data[7:0] / GPIO_P6[7:0] / SD Interface / MC7[5:4],MC6[4,5,3:0] / 8051B_P6[7:0] / COM3	IDE_PDD[7] / GPIO_P6[7] / SD_WP / MC7[5] / 8051B_GPIO_P6[7] / CTS3#, IDE_PDD[6] / GPIO_P6[6] / SD_CD / MC7[4] / 8051B_GPIO_P6[6] / DSR3#, IDE_PDD[5] / GPIO_P6[5] / SD_DATA[1] / MC6[4] / 8051B_GPIO_P6[5] / DTR3#, IDE_PDD[4] / GPIO_P6[4] / SD_DATA[0] / MC6[5] / 8051B_GPIO_P6[4] / SIN3, IDE_PDD[3] / GPIO_P6[3] / SD_CLK / MC6[3] / 8051B_GPIO_P6[3] / RI3#, IDE_PDD[2] / GPIO_P6[2] / SD_CMD / MC6[2] / 8051B_GPIO_P6[2] / RTS3#, IDE_PDD[1] / GPIO_P6[1] / SD_DATA[3] / MC6[1] /	8 PINs

Function	Symbol	PIN Sum
	8051B_GPIO_P6[1] / SOUT3, IDE_PDD[0] / GPIO_P6[0] / SD_DATA[2] / MC6[0] / 8051B_GPIO_P6[0] / DCD3#	
Primary IDE Data[15:8] / GPIO P7[7:0] / SD1 Interface / MCB[1:0],MC8[4,5,3:0] / 8051B P7[7:0] / COM4	IDE_PDD[15] / GPIO_P7[7] / SD1_WP / MCB[1] / 8051B_GPIO_P7[7] / CTS4#, IDE_PDD[14] / GPIO_P7[6] / SD1_CD / MCB[0] / 8051B_GPIO_P7[6] / DSR4#, IDE_PDD[13] / GPIO_P7[5] / SD1_DATA[1] / MC8[4] / 8051B_GPIO_P7[5] / DTR4#, IDE_PDD[12] / GPIO_P7[4] / SD1_DATA[0] / MC8[5] / 8051B_GPIO_P7[4] / SIN4, IDE_PDD[11] / GPIO_P7[3] / SD1_CLK / MC8[3] / 8051B_GPIO_P7[3] / RI4#, IDE_PDD[10] / GPIO_P7[2] / SD1_CMD / MC8[2] / 8051B_GPIO_P7[2] / RTS4#, IDE_PDD[9] / GPIO_P7[1] / SD1_DATA[3] / MC8[1] / 8051B_GPIO_P7[1] / SOUT4, IDE_PDD[8] / GPIO_P7[0] / SD1_DATA[2] / MC8[0] / 8051B_GPIO_P7[0] / DCD4#	8 PINs
Primary IDE CTRL1 / GPIO_P8[7:0] / MCB[3:2],MC9[4,5,3:0] / 8051B P8[7:0] / COM9 / LTP CTRL1	IDE_PCS1# / GPIO_P8[7] / MCB[3] / 8051B_GPIO_P8[7] / CTS9# / AFD#, IDE_PCS0# / GPIO_P8[6] / MCB[2] / 8051B_GPIO_P8[6] / DSR9# / ERR#, IDE_PIOW# / GPIO_P8[5] / SD_ACTIVE / MC9[4] / 8051B_GPIO_P8[5] / DTR9# / INIT#, IDE_PIOR# / GPIO_P8[4] / SD1_ACTIVE / MC9[5] / 8051B_GPIO_P8[4] / SIN9 / SLCIN, IDE_PA[2] / GPIO_P8[3] / MC9[3] / 8051B_GPIO_P8[3] / RI9# / ACK#, IDE_PA[1] / GPIO_P8[2] / MC9[2] / 8051B_GPIO_P8[2] / RTS9# / BUSY, IDE_PA[0] / GPIO_P8[1] / MC9[1] / 8051B_GPIO_P8[1] / SOUT9 / PE, IDE_PINT / GPIO_P8[0] / MC9[0] / 8051B_GPIO_P8[0] / DCD9# / SLCT	8 PINs
MTBF, Primary IDE CTRL 2,	MTBF / GPIO_P9[7] / MCB[5] / 8051B_GPIO_P9[7] / WDT_RSTB / PD[7],	8 PINs

Function	Symbol	PIN Sum
USB Device / GPIO_P9[7:0] / MCB[5:4],MCA[4,5,3:0] / 8051B_GPIO_P9[7:0] / WDT_RSTB / LPT DATA[7:0]	IDE_PDRQ / GPIO_P9[6] / MCB[4] / 8051B_GPIO_P9[6] / PD[6], IDE_PIORDY / GPIO_P9[5] / MCA[4] / 8051B_GPIO_P9[5] / PD[5], IDE_PDACK# / GPIO_P9[4] / MCA[5] / 8051B_GPIO_P9[4] / PD[4], IDE_PCBLID# / GPIO_P9[3] / MCA[3] / 8051B_GPIO_P9[3] / PD[3], IDE_PRST# / GPIO_P9[2] / MCA[2] / 8051B_GPIO_P9[2] / PD[2], UD_DP / GPIO_P9[1] / MCA[1] / 8051B_GPIO_P9[1] / PD[1], UD_DM / GPIO_P9[0] / MCA[0] / 8051B_GPIO_P9[0] / PD[0]	
TXD_EN1-2, LPT CTRL(1) / GPIO_PA[7:5]	TXD_EN1 / GPIO_PA[7], TXD_EN2 / GPIO_PA[6], STB# / GPIO_PA[5]	3 PINs
HD Audio / GPIO_PA[4:0] / General Shift Generator, PWM Signal	H_RST# / GPIO_PA[0] / PWM2_GATE, H_SDI / GPIO_PA[1] / GSF_CH0, H_SDO / GPIO_PA[2] / GSF_CH1, H_SYNC / GPIO_PA[3] / GSF_CH2, H_BCLK / GPIO_PA[4] / GSF_CLK	5 PINs
ADC Interface	ADC_AUX[7:0]	8 PINs
SATA Interface	SATA_CLKP, SATA_CLKN, SATA_TXP, SATA_TXN, SATA_RXP, SATA_RXN, DIF1_SATA_PHY_CLK_P, DIF1_SATA_PHY_CLK_N	8 PINs
Ethernet Interface	LINK/ACTIVE, DUPLEX, ISET, TXN, TXP, RXN, RXP	7 PINs
VGA DVO Interface	G_FPD[0] / G_TVD[0], G_FPD[1] / G_TVD[1], G_FPD[2] / G_TVD[2], G_FPD[3] / G_TVD[3], G_FPD[4] / G_TVD[4], G_FPD[5] / G_TVD[5], G_FPD[6] / G_TVD[6], G_FPD[7] / G_TVD[7], G_FPD[8] / G_TVD[8] / G_STRAP[1], G_FPD[9] / G_TVD[9], G_FPD[10] / G_TVD[10], G_FPD[11] / G_TVD[11], G_FPD[12] / G_STRAP[2], G_FPD[13] / G_STRAP[3], G_FPD[14] / G_STRAP[4], G_FPD[15] / G_STRAP[5], G_FPD[23:18], G_FPD[21:16], G_FP1DE / G_TVDE, G_FP1HS / G_TVHS, G_FP1VS / G_TVVS / G_STRAP[6], G_FP1CLK / G_TVCLKO, G_TVCLKIN, G_FP1DET / G_TVDET, G_CAPD[7:0], G_ENVDD, G_ENBLT, G_ENVEE, G_FP2VS, G_FP2HS,	47 PINs

Function	Symbol	PIN Sum
	G_FP2DET, G_FP2DE, G_FP2CLK, G_CAPCLK	
VGA DAC Interface	G_REXT, G_IOR, G_IOG, G_IOB, G_VSYNC, G_HSYNC, G_DDC_CLK, G_DDC_DAT	8 PINs
VGA GPIO Interface	G_GPIO[2], G_GPIO[3] / G_STRAP[0]	2 PINs
VGA I^2C Interface	G_DDC1_CLK, G_DDC1_DAT, G_DDC2_CLK, G_DDC2_DAT	4 PINs
TEST Pins	TEST	4 PINs
VREF Power	VREF_DDR3DQ075, VREF_DDR3CA075	2 PINs
VGA Power	VDD_DAC09, AVDD_DACR18, AVSS_DACR18, AVDD_DACG18, AVSS_DACG18, AVDD_DACB18, AVSS_DACB18, AVDD_DACBG18, AVSS_DACBG18	9 PINs
PCIe Power	AVDD_PE33, AVDD_PE12, AVDD1_PE12, AVDD_PERX12, AVSS_PERX12, AVDD1_PERX12, AVSS1_PERX12, AVSS_PEPLL12 (2 PINs), AVDD_PEPLL12	12 PINs
SATA Power	AVSS_SATA, AVDD_SATA12, AVSS_SATARX12, AVDD_SATARX12, AVDD_SATAPLL12, AVSS_SATAPLL12, AVDD_SATA33	7 PINs
Ethernet Power	AVDD_EPHYPLL18, AVSS_EPHYPLL18, AVDD_EPHYBG18, AVSS_EPHYBG18, AVDD_EPHYRX18, AVSS_EPHYRX18, AVSS_EPHYTX18, VDD_EPHY18, VSS_EPHY18, VDD_EPHYDL12, VSS_EPHYDL12	11 PINs
USB Power	AVDD_USB33, AVSS_USB33, AVDD1_USB33, AVSS1_USB33, AVDD2_USB33, AVSS2_USB33, AVDD3_USB33, AVSS3_USB33, AVDD_USBBAS33, AVSS_USBBAS33, AVDD2_USBBAS33, AVSS2_USBBAS33, AVDD_USB12, AVDD1_USB12, AVDD2_USB12, AVDD3_USB12, AVDD_USBPLL12, AVSS_USBPLL12, AVDD1_USBPLL12, AVSS1_USBPLL12, AVDD2_USBPLL12, AVSS2_USBPLL12, AVDD3_USBPLL12, AVSS3_USBPLL12	24 PINs
ADC Power	AVDD_ADCVREFP33, AVSS_ADCVREFN33, AVDD_ADC33, AVSS_ADC33, VDD_ADC33, VSS_ADC33, AVDD_TEMP18, AVSS_TEMP18, VDD_TEMP18, VSS_TEMP18, AVDD_PLL18, AVSS_PLL18, AVDD_PLL18, AVSS_PLL18	14 PINs

Function	Symbol	PIN Sum
Battery Power	VDD_BAT, VSS_BAT	2 PINs
Vcore Power	VDD09 (12 PINs)	12 PINs
1.2V Power	VDD12 (8 PINs), VDD_DIF12 (4 PINs), VSS_DIF12 (4 PINs)	16 PINs
1.5V Power	VDD15 (18 PINs)	18 PINs
1.8V Power	VDD18 (8 PINs), VDD_SB18 (4 PINs), AVDD_DDRPHYPLL18, AVSS_DDRPHYPLL18, AVDD_NBVGAPLL18, AVSS_NBVGAPLL18, AVDD_NBDDRPLL18, AVSS_NBDDRPLL18, AVDD_NBCPUPLL18, AVSS_NBCPUPLL18, AVDD_NBTEMP18, AVSS_NBTEMP18	22 PINs
3.3V Power	VDD33 (9 PINs)	9 PINs
Digital Ground	VSS (157 Pins)	157 PINs
NC pin	NC (4 PINs)	4 PINs

5.2. Signal Description

This chapter provides a detailed description of SoC signals. A signal with the symbol "#" at the end of itself indicates that this pin is low active. Otherwise, it is high active.

The following notations are used to describe the signal types:

- **System (7 PINs)**

PIN No.	Symbol	Type	Description
H3	PWRGOOD	I	***Power-Good Input.*** This signal comes from Power Good of the power supply to indicate that the power is available. The SoC uses this signal to generate reset sequence for the system.
AB30	CLK25MOUT	O	***25MHz Clock output.***
AD30	CLK24MOUT	O	***24MHz Clock output***
AK21	XOUT_14318	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator).
AK22	XIN_14318	I	***Crystal-in.*** 14.318MHz frequency input, within 20 ppm tolerance, to the amplifier (oscillator).
AB29	SPEAKER	O	***Speaker Output.*** This pin is used to control the Speaker Output and should be connected to the Speaker. It should be pulled low.
A2	PCIRST#	O	***PCI Reset***. The 1.8V PCI Reset pin, is used to reset PCI devices. When it is asserted low, all the PCI devices will be reset.

- **Test Pin - Internal Connection between North Bridge and South Bridge (2 PINs)**

PIN No.	Symbol	Type	Description
F6	I_XIN_25M	O	***Internal 25MHz Clock Output*** This signal is used to bypass internal 25MHz System Clock for testing usage.
H6	G_XIN_14318	O	***Internal 14.318MHz Clock Output*** This signal is used to bypass internal GPU 14.318MHz Clock for testing usage.

- **DDR3 Interface (78 PINs)**

PIN No.	Symbol	Type	Description
AG20	DRAMRST#	O	***Active Low Asynchronous Reset.*** Reset is active when RESET# is LOW, and otherwise. RESET# must be set as HIGH during normal operation.
AK12 AH13	DRAMCLK DRAMCLK1	O	***Clock output.*** This pin provides the fundamental timing for the DRAM Controller.
AK13 AG13	DRAMCLK# DRAMCLK#1	O	***Clock output.*** This pin provides the fundamental timing for the DRAM controller.
AH14	RAS#	O	***Row Address Strobe.*** When asserted, this signal latches row address on positive edge of the DRAM clock. This signal also allows row access and pre-charge.
AE13	CAS#	O	***Column Address Strobe.*** When asserted, this signal latches column address on the positive edge of the DRAM clock. This signal also allows column access and pre-charge.
AK15	WE#	O	***Memory Write Enable.*** This pin is used as a write enable for the memory data bus.
AJ14 AF14	CKE CKE1	O	***Clock Enable.*** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers.
AK16 AG15	CS0# CS1#	O	***Chip Select CS0# & CS1#.*** These two pins activate the DRAM devices. First Bank of DRAM accepts any command when the CS0# pin is active low. Second Bank of DRAM accepts any command when the CS1# pin is active low.
AH9, AJ9, AH3, AJ1	DQM[3:0]	O	***Data Mask DQM[3:0].*** These pins act as synchronized output enables during read cycles and byte masks during write cy-

PIN No.	Symbol	Type	Description
			cles.
AH10, AK7, AG5, AG1	DQS[3:0]	I/O	***Data Strobe DQS[3:0] for DRAM.*** Output with write data, input with the read data for source synchronous operation.
AG9, AK8, AH4, AH1	DQS#[3:0]	I/O	***Data Strobe DQS#[3:0] for DRAM.*** Output with write data, input with the read data for source synchronous operation.
AK14	ODT[0]	O	***On Die Termination Control for DRAM.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR3 SDRAM.
AF13	ODT[1]	O	***On Die Termination Control for DRAM.*** ODT(registered HIGH) enables on die termination resistance internal to the DDR3 SDRAM.
AA12	ZQ	O	***Reference Voltage for DDR3 only.*** Reference Pin for ZQ calibration
AG16, AE15, AJ16	BA[2:0]	O	***Bank Address BA[2:0].*** These pins are connected to DDR3 as bank address pins.
AF12, AG11, AF7, AF8, AH12, AH8, AG7, AF10, AK11, AJ11, AJ10, AK9, AJ7, AJ6, AK5, AK4, AG6, AF5, AE6, AH6, AE5, AE4, AF3, AG3, AJ4, AJ3, AK2, AJ2, AF1, AE3, AE2, AE1	MD[31:0]	I/O	***Memory Data MD[31:0].*** These pins are connected to the DDR3 data bus.
AF15, AG19, AF20, AK18, AH20, AJ15, AJ20, AF18, AK19, AF17, AJ19, AF16,	MA[15:0]	O	***Memory Address MA[15:0].*** Normally, these pins are used as the row and column address for DDR3.

PIN No.	Symbol	Type	Description
AJ18, AG18, AH17, AK17			

- **USB Interface (12 PINs)**

PIN No.	Symbol	Type	Description
L29 L30	USB_DP USB_DM	I/O	Universal Serial Bus Controller 0 Port 0. These are the serial data pair for USB Port 0. 15kΩ pull down resistors are connected to DP and DM internally.
H29 H30	USB1_DP USB1_DM	I/O	Universal Serial Bus Controller 0 Port 1. These are the serial data pair for USB Port 1. 15kΩ pull down resistors are connected to DP and DM internally.
E29 E30	USB2_DP USB2_DM	I/O	Universal Serial Bus Controller 1 Port 0. These are the serial data pair for USB Port 2. 15kΩ pull down resistors are connected to DP and DM internally.
B29 B30	USB3_DP USB3_DM	I/O	Universal Serial Bus Controller 1 Port 1. These are the serial data pair for USB Port 3. 15kΩ pull down resistors are connected to DP and DM internally.
M28	USB_REXT	I	Universal Serial Bus Controller 0 External Reference Resistance 12kΩ ±1%
K28	USB_REXT1	I	Universal Serial Bus Controller 1 External Reference Resistance 12kΩ ±1%
F28	USB_REXT2	I	Universal Serial Bus Controller 2 External Reference Resistance 12kΩ ±1%
D28	USB_REXT3	I	Universal Serial Bus Controller 3 External Reference Resistance 12kΩ ±1%

- **ISA Bus Interface (87 PINs)**

PIN No.	Symbol	Type	Description
W27	IOCHCK#	I	***I/O Channel Check.*** Provides the system board with parity (error) information about memory or devices on the I/O channel.
Y20	IOCHRDY	I/O	***ISA System Ready.*** This input signal is used to extend the ISA command width for the CPU and DMA cycles.
Y25	AEN	O	***ISA Address Enable.*** This active high output indicates that the system address is enabled during the DMA refresh cycles.
AF24	0WS#	I	***ISA Zero Wait State.*** This is the ISA device zero-wait state indicator signal. This signal terminates the CPU ISA command immediately.
AG26	MEMR#	I/O	***ISA Memory Read.*** This signal is an input during ISA master

PIN No.	Symbol	Type	Description
			cycle.
AB25	MEMW#	I/O	***ISA Memory Write.*** This signal is an input during ISA master cycle. The input is used for redundant slave.
V20	SMEMR#	O	***ISA System Memory Read.*** This signal indicates that the memory read cycle is for an address below 1-MByte address.
Y27	SMEMW#	O	***ISA System Memory Write.*** This signal indicates that the memory write cycle is for an address below 1-MByte address.
N21	IOW#	O	***ISA I/O Write.*** This signal is an input during ISA master cycle.
P21	IOR#	O	***ISA I/O Read.*** This signal is an input during ISA master cycle.
Y26	REFRESH#	O	**Refresh cycle indicator**. ISA master uses this signal to notify DRAM needs refresh. During the memory controller's self-acting refresh cycle, M6117D drives this signal to the I/O channels.
AA25	SYSCLK	O	***System Clock Output***. This signal clocks the ISA bus.
W20	TC	O	***DMA End of Process.*** This is the DMA channel terminal count indicating signal.
AC25	BALE	O	***Bus address Latch Enable***. BALE indicates the presence of a valid address at I/O slots.
V21	SBHE#	I/O	***ISA Bus High Enable.*** In master cycle, it is an input polarity signal and is driven by the master device.The input is used for redundant slave.
U20	MEMCS16#	I/O	***ISA 16-bit Memory Device Select Indicator Signal.***
U25	IOCS16#	I/O	***ISA 16-bit I/O Device Select Indicator Signal.***
AE24	OSC14318	O	14.318MHz Clock Out.
U28	RST_DRV	O	***ISA Reset.*** This output signal is driven active during system power up.
AB27, AC28 AC26, U27, AB26, AE22, AA28, Y28, W25, AF22, AG23	IRQ[15:14], IRQ[12:9], IRQ[7:3]	I	***Interrupt Request Signals***. These are interrupt request input signals.

PIN No.	Symbol	Type	Description
AC27, W21, AE26 Y21, AE23, AF26, AD26	DRQ[7:5], DRQ[3:0]	I	***DMA Device Request.*** These are DMA request input signals.
AE25, U26, AF23 AA29, AG25, AH25, T27	DACK#[7:5], DACK#[3:0]	O	***DMA Device Acknowledge Signals***. These are DMA acknowledge demultiplex select signals. Input function is for hardware setting.
W26, AA27, V27, AE21, AH21, AG21, AH22, AG22, AK23, AJ21, AH23, AJ23, AH24, AG24, AK24, AJ24	SD[15:0]	I/O	***ISA High and Low Byte Slot Data Bus.*** These are the system data lines. These signals read data and vectors into CPU during memory or I/O read cycles or interrupt acknowledge cycles and outputs data from CPU during memory or I/O write cycles.
AG30, AG29, AD27, AF28, AH30, AJ29, AF27, AK29, AG28, AJ30, AG27, AJ28, AH28, AK28, AJ27, AH26, AK27, AK25, AJ26, AK26	SA[19:0]	I/O	***ISA Slot Address Bus.*** These signals are high impedance during hold acknowledge.
AC29, AE29, AD28, AE30, AF29, AE28, AF30	LA[23:17]	O	***ISA Latched Address Bus.***

- **Chip Selection Interface (2 PINs)**

PIN No.	Symbol	Type	Description
V26	GPCS0#	O	***General-Purpose Chip Select 0***.
	STRAP_PLL	I	***PLL Mode Select.*** Pull it high to select Normal mode. Default internal pull-high. Pull it low to test mode. Please set STRAP_PLL pull-high when South Bridge Function [0] 48h[7] and South Bridge Function[0] C0h[30] set to 1. Others setting need pull STRAP_PLL to low.
AD25	GPCS1#	O	***General-Purpose Chip Select 1.***
	STRAP_PLL1_SEL	I	***PLL 14.318MHz Clock Source Select.*** Must pull it low to select 14.318Mhz clock source from XIN_14318.

- **SPI Interface & Hardware strap (4 PINs)** **The SPI function here is to test embedded SPI Flash only.**

Ball No.	Symbol	Type	Description
K11	SPI_CS#	O	***SPI Chip Select.***
	ROM_CS#	O	***ROM Chip Select.*** This pin is used as a ISA ROM chip select.
	STRAP_BMS	I	***Boot Mode Select.*** Pull it high to select Normal boot (Reset 250ms). Default internal pull-high. Pull it low to select Fast boot.
L10	SPI_CK	O	***SPI Clock.***
	STRAP_ JTAG	I	***JTAG Enable.*** Pull it high to enable JTAG. default internal pull-high
L11	SPI_DO	O	***SPI Data Output / Output pin,*** connected with input of flash.
	STRAP_FLASH_SEL	I	***Flash Select.*** Pull it high to select Internal SPI (default internal pull-high) Pull it low to select flash-8bits
K10	SPI_DI	I	***SPI Data Input / Input pin,*** connected with output of flash.

- **Redundant (4 PINs)**

PIN No.	Symbol	Type	Description
W28	EXTSYSFAILIN#	I	***External system fail input.*** This pin is the system fail in for redundant.
AA30	SYSFAILOUT#	O	***System fail output.*** This pin is the system fail out for redundant.
Y29	EXT_SWITCH_FAIL#	I	***External switch fail.*** This pin is the switch input for redundant.
U21	EXT_GPCS#	I	***External GPCS input.*** This pin is the GPCS in for redundant.

- **KBD/MOUSE Interface (4 PINs)**

PIN No.	Symbol	Type	Description
C8	KBCLK	I/O	***Keyboard Clock.*** This pin is keyboard clock when used internal 8042.
	KBRST#	I	***Keyboard Reset.*** This pin is Keyboard reset when used external 8042.
D8	KBDAT	I/O	***Keyboard Data.*** This pin is keyboard data when used internal 8042.
	A20GATE#	I	***Address Bit 20 Mask.*** This pin is A20 mask when used external 8042.
C9	MSCLK	I/O	***Mouse Clock.*** This pin is mouse clock when used internal 8042.
D9	MSDAT	I/O	***Mouse Data.*** This pin is mouse data when used internal 8042.

- **RTC Interface (3 PINs)**

PIN No.	Symbol	Type	Description
C7	RTC_PS	I	***RTC Battery Power Sense.***
B7	RTC_XOUT	O	***Crystal-out***. Frequency output from the inverting amplifier (oscillator)
A7	RTC_XIN	I	***Crystal-in.*** 32.768KHz frequency input, within 20 ppm tolerance, to the amplifier (oscillator).

- **PCIe Bus Interface (16 PINs)**

PIN No.	Symbol	Type	Description
A24 B24	PE_RXP PE_RXN	I	PCIe Differential serial data input. P: positive; N:negative
A22 B22	PE_TXP PE_TXN	O	PCIe Differential serial data output. P: positive; N: negative
A26 B26	PE1_RXP PE1_RXN	I	PCIe Differential serial data input. P: positive; N: negative
C27 D27	PE1_TXP PE1_TXN	O	PCIe Differential serial data output. P: positive; N: negative
E25 E24	PE_CLKP PE_CLKN	I	PCIe Differential reference clock. P: positive; N: negative
D23 D22	DIF_PE_PLLCLK 100_P DIF_PE_PLLCLK 100_N	O	PCIe Differential Clock 100MHz from Internal PLL P: positive; N: negative
A19 B19	DIF_PE_CLK100 _P DIF_PE_CLK100 _N	O	PCIe Differential Clock 100MHz to Port1 P: positive; N: negative
A17 B17	DIF1_PE_CLK10 0_P DIF1_PE_CLK10 0_N	O	PCIe Differential Clock 100MHz to Port2 P: positive; N: negative

- **SPI Embedded Flash Control (2 PINs)**

PIN No.	Symbol	Type	Description
F5	SPIFL_WP#	I/O	***Write- protect pin of SPI embedded flash***, must pull high to 1.8V by a 4.7K ohm resistor.
M10	SPIFL_Hold#	I/O	***Hold pin of SPI embedded flash***, must pull high to 1.8V by a 4.7K ohm resistor.

- **JTAG Interface (4 PINs)**

PIN No.	Symbol	Type	Description
D2	TDO	O	***TDO:*** JTAG Test Data Output pin.
C3	TMS	I	***TMS:*** JTAG Test Mode Select pin.
C2	TCK	I	***TCK:*** JTAG Test Clock Input pin.
D3	TDI	I	***TDI:*** JTAG Test Data Input pin.

- **COM5 / GPIO_P0[7:0] / 8051A_P0[7:0] / MC3[1:0],MC0[4,5,3:0] / 8051B_P0[7:0] / 8051B[SOUT1,SIN1,TXD_EN1,TXD_EN2], FD_SPI2 (8 PINs)**

PIN No.	Symbol	Type	Description
L27	CTS5#	I	***Clear to Send***. This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS#.
	GPIO_P0[7]	I/O	***General-Purpose Input/Output Port 0 [7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[7]	I/O	***8051A General-Purpose Input/Output Port 0[7].***
	MC3[1]	I/O	***Motion Controller 3 [1].***
	8051B_GPIO_P0[7]	I/O	***8051B General-Purpose Input/Output Port 0[7].***
	8051B_SOUT1	O	***8051B COM1 Transmit Data.***
L26	DSR5#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. **Note**: *Bit 5 of the MSR is the complement of **DSR#**.*

PIN No.	Symbol	Type	Description
	GPIO_P0[6]	I/O	***General-Purpose Input/Output Port 0 [6].***This pin can be programmed input or output individually.
	8051A_GPIO_P0[6]	I/O	***8051A General-Purpose Input/Output Port 0[6].***
	MC3[0]	I/O	***Motion Controller 3 [0].***
	8051B_GPIO_P0[6]	I/O	***8051B General-Purpose Input/Output Port 0[6].***
	8051B_SIN1	I	***8051B COM1 Receive Data.***
P27	DTR5#	O	***Data Terminal Ready***. This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P0[5]	I/O	***General-Purpose Input/Output Port 0 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[5]	I/O	***8051A General-Purpose Input/Output Port 0[5].***
	MC0[4]	I/O	***Motion Controller 0 [4].***
	8051B_GPIO_P0[5]	I/O	***8051B General-Purpose Input/Output Port 0[5]***.
	8051B_TXDEN1	I/O	***8051B COM1 TX Status***. This pin will be high when 8051B COM1 is transmitting.
J26	SIN5	I	***COM5 Receive Data***. FIFO UART receiver serial data input signal.
	GPIO_P0[4]	I/O	***General-Purpose Input/Output Port 0 [4]***. This pin can be programmed input or output individually.
	8051A_GPIO_P0[4]	I/O	***8051A General-Purpose Input/Output Port 0[4]***.
	MC0[5]	I/O	***Motion Controller 0 [5]***.
	8051B_GPIO_P0[4]	I/O	***8051B General-Purpose Input/Output Port 0[4]***.
	8051B_TXDEN2	I/O	***8051B COM2 TX Status***. This pin will be high when 8051B COM2 is transmitting.
N27	RI5#	I	***Ring Indicator***. This active low input is for the UART ports. A

PIN No.	Symbol	Type	Description
			handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. **Note**: *Bit 6 of the MSR is the complement of **RI#**.*
	GPIO_P0[3]	I/O	***General-Purpose Input/Output Port 0 [3]***. This pin can be programmed input or output individually.
	8051A_GPIO_P0[3]	I/O	***8051A General-Purpose Input/Output Port 0[3]***.
	MC0[3]	I/O	***Motion Controller 0[3]***.
	8051B_GPIO_P0[3]	I/O	***8051B General-Purpose Input/Output Port 0[3]***.
	FD_SPI2_DI	I	***Full Duplex SPI 2 Data Input t it*** connects to device SDO output.
M25	RTS5#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P0[2]	I/O	***General-Purpose Input/Output Port 0 [2].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[2]	I/O	***8051A General-Purpose Input/Output Port 0[2].***
	MC0[2]	I/O	***Motion Controller 0 [2].***
	8051B_GPIO_P0[2]	I/O	***8051B General-Purpose Input/Output Port 0[2].***
	FD_SPI2_DO	O	***Full Duplex SPI 2 Data Output. It connects to device SDI input.***
M26	SOUT5	O	***COM5 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.

PIN No.	Symbol	Type	Description
	GPIO_P0[1]	I/O	***General-Purpose Input/Output Port 0 [1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[1]	I/O	***8051A General-Purpose Input/Output Port 0[1].***
	MC0[1]	I/O	***Motion Controller 0 [1].***
	8051B_GPIO_P0[1]	I/O	***8051B General-Purpose Input/Output Port 0[1].***
	FD_SPI2_CLK	O	***Full Duplex SPI 2 Clock.***
N25	DCD5#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. **Note:** Bit 7 of the MSR is the complement of DCD#.
	GPIO_P0[0]	I/O	***General-Purpose Input/Output Port 0 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P0[0]	I/O	***8051A General-Purpose Input/Output Port 0[0].***
	MC0[0]	I/O	***Motion Controller 0[0].***
	8051B_GPIO_P0[0]	I/O	***8051B General-Purpose Input/Output Port 0[0].***
	FD_SPI2_CS#	O	***Full Duplex SPI 2 Chip Select.***

- **COM6 / GPIO_P1[7:0] / 8051A_P1[7:0] / MC3[3:2],MC1[4,5,3:0] / 8051B_P1[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
B6	CTS6#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. **Note:** Bit 4 of the MSR is the complement of CTS#.
	GPIO_P1[7]	I/O	***General-Purpose Input/OutputPort1 [7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[7]	I/O	***8051A General-Purpose Input/Output Port1[7].***
	MC3[3]	I/O	***Motion Controller 3[3].***
	8051B_GPIO_P1[7]	I/O	***8051B General-Purpose Input/Output Port1[7].***
D6	DSR6#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. **Note:** Bit 5 of the MSR is the complement of **DSR#**.
	GPIO_P1[6]	I/O	***General-Purpose Input/OutputPort1 [6].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[6]	I/O	***8051A General-Purpose Input/Output Port 1[6].***
	MC3[2]	I/O	***Motion Controller 3 [2].***
	8051B_GPIO_P1[6]	I/O	***8051B General-Purpose Input/Output Port 1[6].***

PIN No.	Symbol	Type	Description
E8	DTR6#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P1[5]	I/O	***General-Purpose Input/Output Port1 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[5]	I/O	***8051A General-Purpose Input/Output Port1[5].***
	MC1[4]	I/O	***Motion Controller 1 [4].***
	8051B_GPIO_P1[5]	I/O	***8051B General-Purpose Input/Output Port1[5].***
A6	SIN6	I	***COM6 Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P1[4]	I/O	***General-Purpose Input/Output Port1 [4].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[4]	I/O	***8051A General-Purpose Input/Output Port1[4].***
	MC1[5]	I/O	***Motion Controller 1 [5].***
	8051B_GPIO_P1[4]	I/O	***8051B General-Purpose Input/Output Port1[4].***
C6	RI6#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	GPIO_P1[3]	I/O	***General-Purpose Input/Output Port1 [3].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[3]	I/O	***8051A General-Purpose Input/Output Port1[3].***
	MC1[3]	I/O	***Motion Controller 1 [3].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P1[3]	I/O	***8051B General-Purpose Input/Output Port1[3].***
F7	RTS6#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
	GPIO_P1[2]	I/O	***General-Purpose Input/Output Port1 [2].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[2]	I/O	***8051A General-Purpose Input/Output Port1[2].***
	MC1[2]	I/O	***Motion Controller 1 [2].***
	8051B_GPIO_P1[2]	I/O	***8051B General-Purpose Input/Output Port1[2].***
E6	SOUT6	O	***COM5 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P1[1]	I/O	***General-Purpose Input/Output Port1 [1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[1]	I/O	***8051A General-Purpose Input/Output Port1[1].***
	MC1[1]	I/O	***Motion Controller 1 [1].***
	8051B_GPIO_P1[1]	I/O	***8051B General-Purpose Input/Output Port1[1].***
D4	DCD6#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

PIN No.	Symbol	Type	Description
	GPIO_P1[0]	I/O	***General-Purpose Input/Output Port1 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P1[0]	I/O	***8051A General-Purpose Input/Output Port1[0].***
	MC1[0]	I/O	***Motion Controller 1 [0].***
	8051B_GPIO_P1[0]	I/O	***8051B General-Purpose Input/Output Port 1[0].***

- **COM7 / GPIO_P2[7:0] / 8051A_P2[7:0] / MC3[5:4],MC2[4,5,3:0] / 8051B_P2[7:0] / SA[31:24] (8 PINs)**

PIN No.	Symbol	Type	Description
K19	CTS7#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	GPIO_P2[7]	I/O	***General-Purpose Input/Output Port2[7].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[7]	I/O	***8051A General-Purpose Input/Output Port2[7].***
	MC3[5]	I/O	***Motion Controller 3 [5].***
	8051B_GPIO_P2[7]	I/O	***8051B General-Purpose Input/Output Port 2[7].***
	ISA_SA[31]	I/O	***ISA Extension Address bit 31***

PIN No.	Symbol	Type	Description
K20	DSR7#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	GPIO_P2[6]	I/O	***General-Purpose Input/OutputPort2 [6].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[6]	I/O	***8051A General-Purpose Input/Output Port 2[6].***
	MC3[4]	I/O	***Motion Controller 3 [4].***
	8051B_GPIO_P2[6]	I/O	***8051B General-Purpose Input/Output Port 2[6].***
	ISA_SA[30]	I/O	***ISA Extension Address bit 30***
E27	DTR7#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	GPIO_P2[5]	I/O	***General-Purpose Input/Output Port2 [5].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[5]	I/O	***8051A General-Purpose Input/Output Port 2[5].***
	MC2[4]	I/O	***Motion Controller 2 [4].***
	8051B_GPIO_P2[5]	I/O	***8051B General-Purpose Input/Output Port 2[5].***
	ISA_SA[29]	I/O	***ISA Extension Address bit 29***
F26	SIN7	I	***COM7 Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P2[4]	I/O	***General-Purpose Input/Output Port2 [4].*** This pin can be programmed input or output individually.

PIN No.	Symbol	Type	Description
	8051A_GPIO_P2[4]	I/O	***8051A General-Purpose Input/Output Port2[4].***
	MC2[5]	I/O	***Motion Controller 2 [5].***
	8051B_GPIO_P2[4]	I/O	***8051B General-Purpose Input/Output Port2[4].***
	ISA_SA[28]	I/O	***ISA Extension Address bit 28***
E26	RI7#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
	GPIO_P2[3]	I/O	***General-Purpose Input/Output Port 2 [3].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[3]	I/O	***8051A General-Purpose Input/Output Port 2[3].***
	MC2[3]	I/O	***Motion Controller 2 [3].***
	8051B_GPIO_P2[3]	I/O	***8051B General-Purpose Input/Output Port 2[3].***
	ISA_SA[27]	I/O	***ISA Extension Address bit 27***
E23	RTS7#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.
	GPIO_P2[2]	I/O	***General-Purpose Input/Output Port 2[2].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[2]	I/O	***8051A General-Purpose Input/Output Port1[2].***
	MC2[2]	I/O	***Motion Controller 2 [2].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P2[2]	I/O	***8051B General-Purpose Input/Output Port 2[2].***
	ISA_SA[26]	I/O	***ISA Extension Address bit 26***
F22	SOUT7	O	***COM7 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P2[1]	I/O	***General-Purpose Input/Output Port 2[1].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[1]	I/O	***8051A General-Purpose Input/Output Port 2[1].***
	MC2[1]	I/O	***Motion Controller 2 [1].***
	8051B_GPIO_P2[1]	I/O	***8051B General-Purpose Input/Output Port 2[1].***
	ISA_SA[25]	I/O	***ISA Extension Address bit 25***
K21	DCD7#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	GPIO_P2[0]	I/O	***General-Purpose Input/Output Port 2 [0].*** This pin can be programmed input or output individually.
	8051A_GPIO_P2[0]	I/O	***8051A General-Purpose Input/Output Port 2[0].***
	MC2[0]	I/O	***Motion Controller 2 [0].***
	8051B_GPIO_P2[0]	I/O	***8051B General-Purpose Input/Output Port 2[0].***
	ISA_SA[24]	I/O	***ISA Extension Address bit 24***

- **Ext RTC / GPIO_P3[7-4] / 8051A_P3[7:4] / TX_DEN[4:3],8051B_P3[5:4] / COM8[CTS,DSR,DTR,SIN] / I^2C1, I^2C (4 PINs)**

PIN No.	Symbol	Type	Description
E1	RTC_AS	O	***RTC Address Strobe.*** This pin is used as the RTC Address

PIN No.	Symbol	Type	Description
			Strobe and should be connected to the RTC.
	GPIO_P3[7]	I/O	***General-Purpose Input/Output Port 3 bit 7.***
	8051A_GPIO_P3[7]	I/O	***8051A General-Purpose Input/Output Port 3 bit 7.***
	TXD_EN4	O	***COM4 TX Status.*** This pin will be high when COM4 is transmitting.
	CTS8#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	I2C1_SDA	I/O	***I2C1 Serial Data.***
G1	RTC_RD#	O	***RTC Read Command.*** This pin is used as the RTC Read Command and should be connected to the RTC.
	GPIO_P3[6]	I/O	***General-Purpose Input/Output Port 3 bit 6.***
	8051A_GPIO_P3[6]	I/O	***8051A General-Purpose Input/Output Port 3 bit 6.***
	TXD_EN3	O	***COM3 TX Status.*** This pin will be high when COM3 is transmitting.
	DSR8#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR#.*
	I2C1_SCL	I/O	***I2C1 Serial Clock.***
G2	RTC_WR#	O	***RTC Write Command.*** This pin is used as the RTC Write Command and should be connected to the RTC.

PIN No.	Symbol	Type	Description
	GPIO_P3[5]	I/O	***General-Purpose Input/Output Port 3 bit 5.***
	8051A_GPIO_P3[5]	I/O	***8051A General-Purpose Input/Output Port 3 bit 5.***
	8051B_SOUT2	O	***8051B COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	8051B_GPIO_P3[5]	I/O	***8051B General-Purpose Input/Output Port 3 bit 5.***
	DTR8#	I	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	I2C_SDA	I/O	***I^2C0 Serial Data.***
B1	RTC_IRQ8#	I	***RTC Interrupt Input.*** This pin is used as the RTC Interrupt input.
	GPIO_P3[4]	I/O	***General-Purpose Input/Output Port 3 bit 4.***
	8051A_GPIO_P3[4]	I/O	***8051A General-Purpose Input/Output Port 3 bit 4.***
	8051B_SIN2	I	***8051B COM2 Receive Data.*** FIFO UART receiver serial data input signal.
	8051B_GPIO_P3[4]	I/O	***8051B General-Purpose Input/Output Port 3 bit 4.***
	SIN8	I/O	***COM8 Receive Data.*** FIFO UART receiver serial data input signal.
	I2C_SCL	I/O	***I^2C0 Serial Clock.***

- **External SPI / GPIO_P3[3-0] / 8051A_P3[3:0] / FD_SPI1 / 8051B_GPIO_P3[3] / COM8[RI,RTS,SOUT,DCD] (4 PINs)**

PIN No.	Symbol	Type	Description
F2	E_SPI_DI	I	***External SPI Data Input,*** it connects to device SDO output.
	GPIO_P3[3]	I/O	***General-Purpose Input/Output Port 3 bit 3***
	8051A_GPIO_P3[3]	I/O	***8051A General-Purpose Input/Output Port 3 bit 3***
	FD_SPI1_DI	I	***Full Duplex SPI 1 Data Input t it connects to device SDO output.***
	8051B_GPIO_P3[3]	I/O	***8051B General-Purpose Input/Output Port 3 bit 3***
	RI8#	I/O	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
C1	E_SPI_DO	O	***External SPI Data Output. It connects to device SDI input.***
	GPIO_P3[2]	I/O	***General-Purpose Input/Output Port 3 bit 2***
	8051A_GPIO_P3[2]	I/O	***8051A General-Purpose Input/Output Port 3 bit 2***
	FD_SPI1_DO	O	***Full Duplex SPI 1 Data Output. It connects to device SDI input.***
	8051B_GPIO_P3[2]	I/O	***8051B General-Purpose Input/Output Port 3 bit 2***
	RTS8#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.

PIN No.	Symbol	Type	Description
F1	E_SPI_CLK	O	***External SPI Clock***
	GPIO_P3[1]	I/O	***General-Purpose Input/Output Port 3 bit 1***
	8051A_GPIO_P3[1]	I/O	***8051A General-Purpose Input/Output Port 3 bit 1***
	FD_SPI1_CLK	O	***Full Duplex SPI 1 SPI Clock.***
	8051B_GPIO_P3[1]	I/O	***8051B General-Purpose Input/Output Port 3 bit 1***
	SOUT8	O	***COM8 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	8051B_SOUT2	O	***8051B COM2 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
D1	E_SPI_CS#	O	***External SPI Chip Select***
	GPIO_P3[0]	I/O	***General-Purpose Input/Output Port 3 bit 0.***
	8051A_GPIO_P3[0]	I/O	***8051A General-Purpose Input/Output Port 3 bit 0.***
	FD_SPI1_CS#	O	***Full Duplex SPI 1 Chip Select.***
	8051B_GPIO_P3[0]	I/O	***8051B General-Purpose Input/Output Port 3 bit 0***
	DCD8#	I/O	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **COM1 / GPIO_P4[7:0] / 8051A_GPIO_P4[7:0] / MC7[1:0],MC4[4,5,3:0] / 8051B_GPIO_P4[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
M21	CTS1#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS1# signal by reading bit 4 of Modem Status Register (MSR). A CTS1# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS1# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS1#.*
	GPIO_P4[7]	I/O	***General-Purpose Input/Output Port 4 bit 7.***
	8051A_GPIO_P4[7]	I/O	***8051A General-Purpose Input/Output Port 4 bit 7.***
	MC7[1]	I/O	***Motion Controller 7 [1].***
	8051B_GPIO_P4[7]	I/O	***8051B General-Purpose Input/Output Port 4 bit 7.***
T26	DSR1#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR1# signal by reading bit5 of the Modem Status Register (MSR). A DSR1# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR1# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR1#.*
	GPIO_P4[6]	I/O	***General-Purpose Input/Output Port 4 bit 6.***
	8051A_GPIO_P4[6]	I/O	***8051A General-Purpose Input/Output Port 4 bit 6.***
	MC7[0]	I/O	***Motion Controller 7 [0].***
	8051B_GPIO_P4[6]	I/O	***8051B General-Purpose Input/Output Port 4 bit 6.***

PIN No.	Symbol	Type	Description
T25	DTR1#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR1# signal to be inactive during the loop-mode operation.
	GPIO_P4[5]	I/O	***General-Purpose Input/Output Port 4 bit 5.***
	8051A_GPIO_P4[5]	I/O	***8051A General-Purpose Input/Output Port 4 bit 5.***
	MC4[4]	I/O	***Motion Controller 4 [4].***
	8051B_GPIO_P4[5]	I/O	***8051B General-Purpose Input/Output Port 4 bit 5.***
N26	SIN1	I	***Receive Data.*** FIFO UART receiver serial data input signal.
	GPIO_P4[4]	I/O	***General-Purpose Input/Output Port 4 bit 4.***
	8051A_GPIO_P4[4]	I/O	***8051A General-Purpose Input/Output Port 4 bit 4.***
	MC4[5]	I/O	***Motion Controller 4 [5].***
	8051B_GPIO_P4[4]	I/O	***8051B General-Purpose Input/Output Port 4 bit 4.***
L21	RI1#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI1# signal by reading bit 6 of the Modem Status Register (MSR). An RI1# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI1# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI1#.*
	GPIO_P4[3]	I/O	***General-Purpose Input/Output Port 4 bit 3.***
	8051A_GPIO_P4[3]	I/O	***8051A General-Purpose Input/Output Port 4 bit 3.***
	MC4[3]	I/O	***Motion Controller 4 [3].***
	8051B_GPIO_P4[3]	I/O	***8051B General-Purpose Input/Output Port 4 bit 3.***

PIN No.	Symbol	Type	Description
R27	RTS1#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.
	GPIO_P4[2]	I/O	***General-Purpose Input/Output Port 4 bit 2.***
	8051A_GPIO_P4[2]	I/O	***8051A General-Purpose Input/Output Port 4 bit 2.***
	MC4[2]	I/O	***Motion Controller 4 [2].***
	8051B_GPIO_P4[2]	I/O	***8051B General-Purpose Input/Output Port 4 bit 2.***
R26	SOUT1	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	GPIO_P4[1]	I/O	***General-Purpose Input/Output Port 4 bit 1.***
	8051A_GPIO_P4[1]	I/O	***8051A General-Purpose Input/Output Port 4 bit 1.***
	MC4[1]	I/O	***Motion Controller 4 [1].***
	8051B_GPIO_P4[1]	I/O	***8051B General-Purpose Input/Output Port 4 bit 1.***
R28	DCD1#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD1# signal by reading bit 7 of the Modem Status Register (MSR). A DCD1# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the in-terrupt is generated when DCD1# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD1#.*
	GPIO_P4[0]	I/O	***General-Purpose Input/Output Port 4 bit 0.***
	8051A_GPIO_P4[0]	I/O	***8051A General-Purpose Input/Output Port 4 bit 0.***
	MC4[0]	I/O	***Motion Controller 4 [0].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P4[0]	I/O	***8051B General-Purpose Input/Output Port 4 bit 0.***

- **PWM / GPIO_P5[7:0] / MC7[3:2],MC5[4,5,3:0] / 8051B_GPIO_P5[7:0] / COM2 (8 PINs)**

PIN No.	Symbol	Type	Description
C11	PWM1_GATE	I	***PWM Timer1 Gate.*** This pin is PWM timer1 gate mask when South Bridge C0[2] is 1 (Pins for PWM).
	GPIO_P5[7]	I/O	***General-Purpose Input/Output Port 5 bit 7.***
	MC7[3]	I/O	***Motion Controller 7 [3].***
	8051B_GPIO_P5[7]	I/O	***8051B General-Purpose Input/Output Port 5 bit 7.***
	CTS2#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS2# signal by reading bit 4 of Modem Status Register (MSR). A CTS2# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS1# changes the state. The CTS2# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS2#.*
D12	PWM_GATE	I	***PWM Timer Gate.*** This pin is PWM timer gate mask when South Bridge register C0h bit2 is 1 (Pins for PWM).
	GPIO_P5[6]	I/O	***General-Purpose Input/Output Port 5 bit 6.***
	MC7[2]	I/O	***Motion Controller 7 [2].***
	8051B_GPIO_P5[6]	I/O	***8051B General-Purpose Input/Output Port 5 bit 6.***
	DSR2#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the DSR2# signal by reading bit5 of the Modem Status Register (MSR). A DSR2# signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DSR2# changes state. ***Note:*** *Bit 5 of the MSR is the complement of DSR2#.*
D11	PWM2_OUT	O	***PWM Timer2 Output.*** This pin is PWM timer1 output when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[5]	I/O	***General-Purpose Input/Output Port 5 bit 5.***

PIN No.	Symbol	Type	Description
	MC5[4]	I/O	***Motion Controller 5 [4].***
	8051B_GPIO_P5[5]	I/O	***8051B General-Purpose Input/Output Port 5 bit 5.***
	DTR2#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR2# signal to be inactive during the loop-mode operation.
D10	PWM2_CLK	I	***PWM Timer2 Clock.*** This pin is PWM timer2 external clock input when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[4]	I/O	***General-Purpose Input/Output Port 5 bit 4.***
	MC5[5]	I/O	***Motion Controller 5 [5].***
	8051B_GPIO_P5[4]	I/O	***8051B General-Purpose Input/Output Port 5 bit 4.***
	SIN2	I	***Receive Data.*** FIFO UART receiver serial data input signal.
D14	PWM1_CLK	I	***PWM Timer1 Clock.*** This pin is PWM timer1 external clock input when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[3]	I/O	***General-Purpose Input/Output Port 5 bit 3.***
	MC5[3]	I/O	***Motion Controller 5 [3].***
	8051B_GPIO_P5[3]	I/O	***8051B General-Purpose Input/Output Port 5 bit 3.***
	RI2#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the RI2# signal by reading bit 6 of the Modem Status Register (MSR). An RI2# signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when RI2# changes state. ***Note:*** *Bit 6 of the MSR is the complement of RI2#.*
D13	PWM1_OUT	O	***PWM Timer1 Output.*** This pin is PWM timer1 output when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[2]	I/O	***General-Purpose Input/Output Port 5 bit 2.***
	MC5[2]	I/O	***Motion Controller 5 [2].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P5[2]	I/O	***8051B General-Purpose Input/Output Port 5 bit 2.***
	RTS2#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTS1# signal to be inactive mode (high). It is forced to be inactive during the loop-mode operation.
D15	PWM_OUT	O	***PWM Timer Output.*** This pin is PWM timer output when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[1]	I/O	***General-Purpose Input/Output Port 5 bit 1.***
	MC5[1]	I/O	***Motion Controller 5 [1].***
	8051B_GPIO_P5[1]	I/O	***8051B General-Purpose Input/Output Port 5 bit 1.***
	SOUT2	O	***Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
E12	PWM_CLK	I	***PWM Timer Clock.*** This pin is PWM timer external clock input when South Bridge C0h[2] is 1 (Pins for PWM).
	GPIO_P5[0]	I/O	***General-Purpose Input/Output Port 5 bit 0.***
	MC5[0]	I/O	***Motion Controller 5 [0].***
	8051B_GPIO_P5[0]	I/O	***8051B General-Purpose Input/Output Port 5 bit 0.***
	DCD2#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD2# signal by reading bit 7 of the Modem Status Register (MSR). A DCD2# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD2# changes state. **Note:** Bit 7 of the MSR is the complement of DCD2#.

- **Primary IDE Data[7:0] / GPIO_P6[7:0] / SD Interface / MC7[5:4],MC6[4,5,3:0] / 8051B_P6[7:0] / COM3 (8 PINs)**

PIN No.	Symbol	Type	Description
K12	IDE_PDD[7]	I/O	***IDE Primary Channel Data Bus Data 7.***
	GPIO_P6[7]	I/O	***General-Purpose Input/Output Port 6[7].*** This pin can be programmed input or output individually.
	SD_WP	I	***SD0 Write Protect.***
	MC7[5]	I/O	***Motion Controller 7 [5].***
	8051B_GPIO_P6[7]	I/O	***8051B General-Purpose Input/Output Port 6[7].***
	CTS3#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
K13	IDE_PDD[6]	I/O	***IDE Primary Channel Data Bus Data 6.***
	GPIO_P6[6]	I/O	***General-Purpose Input/Output Port 6[6].*** This pin can be programmed input or output individually.
	SD_CD	I	***SD0 Card Detect.***
	MC7[4]	I/O	***Motion Controller 7 [4].***
	8051B_GPIO_P6[6]	I/O	***8051B General-Purpose Input/Output Port 6[6].***
	DSR3#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#.***
F3	IDE_PDD[5]	I/O	***IDE Primary Channel Data Bus Data 5.***
	GPIO_P6[5]	I/O	***General-Purpose Input/Output Port 6[5].*** This pin can be programmed input or output individually.

PIN No.	Symbol	Type	Description
	SD_DATA[1]	I/O	***SD0 Data Bus Data 1.***
	MC6[4]	I/O	***Motion Controller 6 [4].***
	8051B_GPIO_P6[5]	I/O	***8051B General-Purpose Input/Output Port 6[5].***
	DTR3#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
E4	IDE_PDD[4]	I/O	***IDE Primary Channel Data Bus Data 4.***
	GPIO_P6[4]	I/O	***General-Purpose Input/Output Port 6[4].*** This pin can be programmed input or output individually.
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
	MC6[5]	I/O	***Motion Controller 6 [5].***
	8051B_GPIO_P6[4]	I/O	***8051B General-Purpose Input/Output Port 6[4].***
	SIN3	I	***COM3 Receive Data.*** FIFO UART receiver serial data input signal.
E3	IDE_PDD[3]	I/O	***IDE Primary Channel Data Bus Data 3.***
	GPIO_P6[3]	I/O	***General-Purpose Input/Output Port 6[3].*** This pin can be programmed input or output individually.
	SD_CLK	O	***SD0 Clock.***
	MC6[3]	I/O	***Motion Controller 6 [3].***
	8051B_GPIO_P6[3]	I/O	***8051B General-Purpose Input/Output Port 6[3].***
	RI3#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*

PIN No.	Symbol	Type	Description
L12	IDE_PDD[2]	I/O	***IDE Primary Channel Data Bus Data 2.***
	GPIO_P6[2]	I/O	***General-Purpose Input/Output Port 6[2].*** This pin can be programmed input or output individually.
	SD_CMD	I/O	***SD0 Command/Response.***
	MC6[2]	I/O	***Motion Controller 6 [2].***
	8051B_GPIO_P6[2]	I/O	***8051B General-Purpose Input/Output Port 6[2].***
	RTS3#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.
F4	IDE_PDD[1]	I/O	***IDE Primary Channel Data Bus Data 1.***
	GPIO_P6[1]	I/O	***General-Purpose Input/Output Port 6[1].*** This pin can be programmed input or output individually.
	SD_DATA[3]	I/O	***SD0 Data Bus Data 3.***
	MC6[1]	I/O	***Motion Controller 6 [1].***
	8051B_GPIO_P6[1]	I/O	***8051B General-Purpose Input/Output Port 6[1].***
	SOUT3	O	***COM3 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
L13	IDE_PDD[0]	I/O	***IDE Primary Channel Data Bus Data 0.***
	GPIO_P6[0]	I/O	***General-Purpose Input/Output Port 6[0].*** This pin can be programmed input or output individually.
	SD_DATA[2]	I/O	***SD0 Data Bus Data 2.***
	MC6[0]	I/O	***Motion Controller 6 [0].***
	8051B_GPIO_P6[0]	I/O	***8051B General-Purpose Input/Output Port 6[0].***

PIN No.	Symbol	Type	Description
	DCD3#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **Primary IDE Data[15:8] / GPIO P7[7:0] / SD1 Interface / MCB[1:0],MC8[4,5,3:0] / 8051B P7[7:0] / COM4 (8 PINs)**

PIN No.	Symbol	Type	Description
C5	IDE_PDD[15]	I/O	***IDE Primary Channel Data Bus Data 15.***
	GPIO_P7[7]	I/O	***General-Purpose Input/Output Port 7[7].*** This pin can be programmed input or output individually.
	SD1_WP	I	***SD1 Write Protect.***
	MCB[1]	I/O	***Motion Controller B [1].***
	8051B_GPIO_P7[7]	I/O	***8051B General-Purpose Input/Output Port 7[7].***
	CTS4#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
D5	IDE_PDD[14]	I/O	***IDE Primary Channel Data Bus Data 14.***
	GPIO_P7[6]	I/O	***General-Purpose Input/Output Port 7[6].*** This pin can be programmed input or output individually.
	SD1_CD	I	***SD1 Card Detect.***
	MCB[0]	I/O	***Motion Controller B [0].***
	8051B_GPIO_P7[6]	I/O	***8051B General-Purpose Input/Output Port 7[6].***
	DSR4#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*

PIN No.	Symbol	Type	Description
A4	IDE_PDD[13]	I/O	***IDE Primary Channel Data Bus Data 13.***
	GPIO_P7[5]	I/O	***General-Purpose Input/Output Port 7[5].*** This pin can be programmed input or output individually.
	SD1_DATA[1]	I/O	***SD1 Data Bus Data 1.***
	MC8[4]	I/O	***Motion Controller 8 [4].***
	8051B_GPIO_P7[5]	I/O	***8051B General-Purpose Input/Output Port 7[5].***
	DTR4#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
B4	IDE_PDD[12]	I/O	***IDE Primary Channel Data Bus Data 12.***
	GPIO_P7[4]	I/O	***General-Purpose Input/Output Port 7[4].*** This pin can be programmed input or output individually.
	SD_DATA[0]	I/O	***SD0 Data Bus Data 0.***
	MC8[5]	I/O	***Motion Controller 8 [5].***
	8051B_GPIO_P7[4]	I/O	***8051B General-Purpose Input/Output Port 7[4].***
	SIN4	I	***COM4 Receive Data.*** FIFO UART receiver serial data input signal.
A3	IDE_PDD[11]	I/O	***IDE Primary Channel Data Bus Data 11.***
	GPIO_P7[3]	I/O	***General-Purpose Input/Output Port 7[3].*** This pin can be programmed input or output individually.
	SD1_CLK	O	***SD1 Clock.***
	MC8[3]	I/O	***Motion Controller 8 [3].***
	8051B_GPIO_P7[3]	I/O	***8051B General-Purpose Input/Output Port 7[3].***

PIN No.	Symbol	Type	Description
	RI4#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#****.*
B3	IDE_PDD[10]	I/O	***IDE Primary Channel Data Bus Data 10.***
	GPIO_P7[2]	I/O	***General-Purpose Input/Output Port 7[2].*** This pin can be programmed input or output individually.
	SD1_CMD	I/O	***SD1 Command/Response.***
	MC8[2]	I/O	***Motion Controller 8 [2].***
	8051B_GPIO_P7[2]	I/O	***8051B General-Purpose Input/Output Port 7[2].***
	RTS4#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.
A5	IDE_PDD[9]	I/O	***IDE Primary Channel Data Bus Data 9.***
	GPIO_P7[1]	I/O	***General-Purpose Input/Output Port 7[1].*** This pin can be programmed input or output individually.
	SD1_DATA[3]	I/O	***SD1 Data Bus Data 3.***
	MC8[1]	I/O	***Motion Controller 8 [1].***
	8051B_GPIO_P7[1]	I/O	***8051B General-Purpose Input/Output Port 7[1].***
	SOUT4	O	***COM4 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
C4	IDE_PDD[8]	I/O	***IDE Primary Channel Data Bus Data 8.***

PIN No.	Symbol	Type	Description
	GPIO_P7[0]	I/O	***General-Purpose Input/Output Port 7[0].*** This pin can be programmed input or output individually.
	SD1_DATA[2]	I/O	***SD1 Data Bus Data 2.***
	MC8[0]	I/O	***Motion Controller 8 [0].***
	8051B_GPIO_P7[0]	I/O	***8051B General-Purpose Input/Output Port 7[0].***
	DCD4#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*

- **Primary IDE CTRL1 / GPIO_P8[7:0] / MCB[3:2],MC9[4,5,3:0] / 8051B P8[7:0] / COM9 / LTP CTRL1 (8 PINs)**

PIN No.	Symbol	Type	Description
F13	IDE_PCS1#	O	***IDE Primary Channel Chip Select.***
	GPIO_P8[7]	I/O	***General-Purpose Input/Output Port 8[7].*** This pin can be programmed input or output individually.
	MCB[3]	I/O	***Motion Controller B [3].***
	8051B_GPIO_P8[7]	I/O	***8051B General-Purpose Input/Output Port 8[7].***
	CTS9#	I	***Clear to Send.*** This active low input for the primary and secondary serial ports. A handshake signal notifies the UART that the modem is ready to receive data. The CPU can monitor the status of the CTS# signal by reading bit 4 of Modem Status Register (MSR). A CTS# signal states the change from low to high after the last MSR read sets bit 0 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when CTS# changes the state. The CTS# signal has no effect on the transmitter. ***Note:*** *Bit 4 of the MSR is the complement of CTS#.*
	AFD#	OD	***AFD#.*** An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F12	IDE_PCS0#	O	***IDE Primary Channel Chip Select.***
	GPIO_P8[6]	I/O	***General-Purpose Input/Output Port 8[6].*** This pin can be programmed input or output individually.
	MCB[2]	I/O	***Motion Controller B [2].***
	8051B_GPIO_P8[6]	I/O	***8051B General-Purpose Input/Output Port 8[6].***

PIN No.	Symbol	Type	Description
	DSR9#	I	***Data Set Ready.*** This active low input is for the UART ports. A handshake signal notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of the **DSR#** signal by reading bit5 of the Modem Status Register (MSR). A **DSR#** signal states the change from low to high after the last MSR read sets bit1 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **DSR#** changes state. ***Note:*** *Bit 5 of the MSR is the complement of* ***DSR#****.*
	ERR#	I	***ERR#.*** An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F11	IDE_PIOW#	O	***IDE Primary Channel I/O Write Strobe.***
	GPIO_P8[5]	I/O	***General-Purpose Input/Output Port 8[5].*** This pin can be programmed input or output individually.
	SD_ACTIVE	O	***SD Read/Write status. High active***
	MC9[4]	I/O	***Motion Controller 9 [4].***
	8051B_GPIO_P8[5]	I/O	***8051B General-Purpose Input/Output Port 8[5].***
	DTR9#	O	***Data Terminal Ready.*** This is an active low output for the UART port. A handshake output signal signifies the modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTR# signal to be inactive during the loop-mode operation.
	INIT#	OD	***INIT#.*** Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
E9	IDE_PIOR#	O	***IDE Primary Channel I/O Read Strobe.***
	GPIO_P8[4]	I/O	***General-Purpose Input/Output Port 8[4].*** This pin can be programmed input or output individually.
	SD1_ACTIVE	O	***SD1 Read/Write status. High active***
	MC9[5]	I/O	***Motion Controller 9 [5].***
	8051B_GPIO_P8[4]	I/O	***8051B General-Purpose Input/Output Port 8[4].***

PIN No.	Symbol	Type	Description
	SIN9	I	***COM9 Receive Data.*** FIFO UART receiver serial data input signal.
	SLCIN	OD	***SLIN#.*** Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
F9	IDE_PA[2]	O	***IDE Primary Channel Device Address***
	GPIO_P8[3]	I/O	***General-Purpose Input/Output Port 8[3].*** This pin can be programmed input or output individually.
	MC9[3]	I/O	***Motion Controller 9 [3].***
	8051B_GPIO_P8[3]	I/O	***8051B General-Purpose Input/Output Port 8[3].***
	ACK#	I	***ACK#.*** An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	RI9#	I	***Ring Indicator.*** This active low input is for the UART ports. A handshake signal notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of the **RI#** signal by reading bit 6 of the Modem Status Register (MSR). An **RI#** signal states the change from low to high after the last MSR read sets bit 2 of the MSR to a “1”. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when **RI#** changes state. ***Note:*** *Bit 6 of the MSR is the complement of* ***RI#.***
F10	IDE_PA[1]	O	***IDE Primary Channel Device Address***
	GPIO_P8[2]	I/O	***General-Purpose Input/Output Port 8[2].*** This pin can be programmed input or output individually.
	MC9[2]	I/O	***Motion Controller 9 [2].***
	8051B_GPIO_P8[2]	I/O	***8051B General-Purpose Input/Output Port 8[2].***

PIN No.	Symbol	Type	Description
	RTS9#	O	***Request to Send.*** Active low Request to Send output for UART port. A handshake output signal notifies the modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hard-ware reset will clear the **RTS#** signal to be inactive mode (high). It is forced to be inactive during the loop-mode opera-tion.
	BUSY	I	***BUSY.*** An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
F8	IDE_PA[0]	O	***IDE Primary Channel Device Address***
	GPIO_P8[1]	I/O	***General-Purpose Input/Output Port 8[1].*** This pin can be programmed input or output individually.
	MC9[1]	I/O	***Motion Controller 9 [1].***
	8051B_GPIO_P 8[1]	I/O	***8051B General-Purpose Input/Output Port 8[1].***
	SOUT9	O	***COM9 Transmit Data.*** FIFO UART transmitter serial data output from the serial port.
	PE	I	***PE.*** An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
E11	IDE_PINT	I	***IDE Primary Channel Interrupt.***
	GPIO_P8[0]	I/O	***General-Purpose Input/Output Port 8[0].*** This pin can be programmed input or output individually.
	MC9[0]	I/O	***Motion Controller 9 [0].***
	8051B_GPIO_P 8[0]	I/O	***8051B General-Purpose Input/Output Port 8[0].***

PIN No.	Symbol	Type	Description
	DCD9#	I	***Data Carrier Detect.*** This active low input is for the UART ports. A handshake signal notifies the UART that the carrier signal is detected by the modem. The CPU can monitor the status of the DCD# signal by reading bit 7 of the Modem Status Register (MSR). A DCD# signal states the change from low to high after the last MSR read sets bit 3 of the MSR to a "1". If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when DCD# changes state. ***Note:*** *Bit 7 of the MSR is the complement of DCD#.*
	SLCT	I	***SLCT.*** An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.

- **MTBF, Primary IDE CTRL 2, USB Device / GPIO_P9[7:0] / MCB[5:4],MCA[4,5,3:0] / 8051B_GPIO_P9[7:0] / WDT_RSTB / LPT DATA[7:0] (8 PINs)**

PIN No.	Symbol	Type	Description
G27	MTBF	O	***MTBF Flag output.***
	GPIO_P9[7]	I/O	***General-Purpose Input/Output Port 9[7].*** This pin can be programmed input or output individually.
	MCB[5]	I/O	***Motion Controller B [5].***
	8051B_GPIO_P9[7]	I/O	***8051B General-Purpose Input/Output Port 9[7].***
	WDT_RSTB	O	***Watchdog 1 Timeout Signal.***
	PD[7]	I/O	***Parallel port data bus bit 7.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
J25	IDE_PDRQ	I	***IDE Primary Channel DMA Request.***
	GPIO_P9[6]	I/O	***General-Purpose Input/Output Port 9[6].*** This pin can be programmed input or output individually.
	MCB[4]	I/O	***Motion Controller B [4].***
	8051B_GPIO_P9[6]	I/O	***8051B General-Purpose Input/Output Port 9[6].***
	PD[6]	I/O	***Parallel port data bus bit 6.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
G26	IDE_PIORDY	I	***IDE Primary Channel I/O Channel Ready.***
	GPIO_P9[5]	I/O	***General-Purpose Input/Output Port 9[5].*** This pin can be programmed input or output individually.
	MCA[4]	I/O	***Motion Controller A [4].***
	8051B_GPIO_P9[5]	I/O	***8051B General-Purpose Input/Output Port 9[5].***
	PD[5]	I/O	***Parallel port data bus bit 5.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
H25	IDE_PDACK#	O	***IDE Primary Channel DMA Acknowledge.***
	GPIO_P9[4]	I/O	***General-Purpose Input/Output Port 9[4].*** This pin can be programmed input or output individually.
	MCA[5]	I/O	***Motion Controller A [5].***

PIN No.	Symbol	Type	Description
	8051B_GPIO_P9[4]	I/O	***8051B General-Purpose Input/Output Port 9[4].***
	PD[4]	I/O	***Parallel port data bus bit 4.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
H27	IDE_PCBLID#	I	***IDE Primary Channel Cable Assembly Type Identifier.***
	GPIO_P9[3]	I/O	***General-Purpose Input/Output Port 9[3].*** This pin can be programmed input or output individually.
	MCA[3]	I/O	***Motion Controller A [3].***
	8051B_GPIO_P9[3]	I/O	***8051B General-Purpose Input/Output Port 9[3].***
	PD[3]	I/O	***Parallel port data bus bit 3.*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
J27	IDE_PRST#	O	***IDE Primary Channel Reset.***
	GPIO_P9[2]	I/O	***General-Purpose Input/Output Port 9[2].*** This pin can be programmed input or output individually.
	MCA[2]	I/O	***Motion Controller A [2].***
	8051B_GPIO_P9[2]	I/O	***8051B General-Purpose Input/Output Port 9[2].***
	PD[2]	I/O	***Parallel port data bus bit 2 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
K26	UD_DP	I/O	***Universal Serial Bus Device Controller Port Data+.*** These are the serial data pair for USB Device. Need add 1.5kΩ pull up resistors to UD_DP externally.
	GPIO_P9[1]	I/O	***General-Purpose Input/Output Port 9[1].*** This pin can be programmed input or output individually.
	MCA[1]	I/O	***Motion Controller A [1].***
	8051B_GPIO_P9[1]	I/O	***8051B General-Purpose Input/Output Port 9[1].***
	PD[1]	I/O	***Parallel port data bus bit 1 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

PIN No.	Symbol	Type	Description
K25	UD_DM	I/O	***Universal Serial Bus Device Controller Data-.*** These are the serial data pair for USB Device.
	GPIO_P9[0]	I/O	***General-Purpose Input/Output Port 9[0].*** This pin can be programmed input or output individually.
	MCA[0]	I/O	***Motion Controller A [0].***
	8051B_GPIO_P9[0]	I/O	***8051B General-Purpose Input/Output Port 9[0].***
	PD[0]	I/O	***Parallel port data bus bit 0 .*** Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

- **TXD_EN1-2, LPT CTRL(1) / GPIO_PA[7:5] (3 PINs)**

PIN No.	Symbol	Type	Description
L14	TX_DEN1	O	***COM1 TX Status.*** This pin will be high when COM1 is trans-mitting.
	GPIO_PA[7]	I/O	***General-Purpose Input/Output Port A[7].*** Those pins can be programmed input or output individually.
K14	TX_DEN2	O	***COM2 TX Status.*** This pin will be high when COM2 is trans-mitting.
	GPIO_PA[6]	I/O	***General-Purpose Input/Output Port A[6].*** Those pins can be programmed input or output individually.
M14	STB#	OD	***STB#.*** An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO_PA[5]	I/O	***General-Purpose Input/Output Port A[5] .*** Those pins can be programmed input or output individually.

- **HD Audio / GPIO_PA[4:0] / General Shift Generator, PWM Signal (5 PINs)**

PIN No.	Symbol	Type	Description
E14	H_BCLK	O	**Global Link 24.00-MHz clock**
	GPIO_PA[4]	I/O	***General-Purpose Input/Output PortA[4].*** Those pins can be programmed input or output individually.
	GSF_CLK	O	***General Shifter reference Clock***
L15	H_SYNC	O	**Global 48 kHz Frame Sync and outbound tag signal**
	GPIO_PA[3]	I/O	***General-Purpose Input/Output PortA[3].*** Those pins can be

PIN No.	Symbol	Type	Description
			programmed input or output individually.
	GSF_CH2	I/O	***General Shifter Channel 2***
F14	H_SDO	O	**Bussed Serial Data Output(s)**
	GPIO_PA[2]	I/O	***General-Purpose Input/Output PortA[2] .*** Those pins can be programmed input or output individually.
	GSF_CH1	I/O	***General Shifter Channel 1***
K16	H_SDI	I/O	**Point-to-point Serial Data Input(s).** Controller has a weak pull down
	GPIO_PA[1]	I/O	***General-Purpose Input/Output Port A[1]*** . Those pins can be programmed input or output individually.
	GSF_CH0	I/O	***General Shifter Channel 0***
F15	H_RST#	O	**Global active low reset**
	GPIO_PA[0]	I/O	***General-Purpose Input/Output Port A[0]*** . Those pins can be programmed input or output individually.
	PWM2_GATE	I	***PWM Timer2 Gate.*** This pin is PWM timer2 gate mask when South Bridge C0h[2] is 1 (Pins for PWM).

- **ADC Interface (8 PINs)**

PIN No.	Symbol	Type	Description
E19, F19, E20, F20, F17, D20, D19, F18	ADC_AUX[7:0]	I	***ADC Analog Input***

- **Serial ATA Interface (8 PINs)**

PIN No.	Symbol	Type	Description
V30 V29	SATA_TXP SATA_TXN	O	***Serial ATA Device Controller TX Port***. These are the serial ATA Transmitter pair for Serial ATA Device.
T30 T29	SATA _RXP SATA _RXN	I	***Serial ATA Device Controller RX Port***. These are the serial ATA Receive pair for Serial ATA Device.
P30 N30	SATA_CLKP SATA_CLKN	I	***Differential PLL Reference Clock Pair.***
A20 B20	DIF0_SATA_PHY_CLK_P DIF0_SATA_PH	O	***Differential Clock Pair from Internal PLL.***

	Y_CLK_N		

- **Ethernet Interface (7 PINs)**

PIN No.	Symbol	Type	Description
G5	LINK/ACTIVE	O	***LINK/ACTIVE.*** Link/active status
G4	DUPLEX	O	***DUPLEX.*** Duplex status
C13	ISET	I	***ISET.*** External resistor 6.02kΩ ±1%connecting pin for BIAS
B12	TXN	O	***TXN.*** 10B-T/100BT transmitting output pin/ receiving input pin (negative)
A12	TXP	O	***TXP.*** 10B-T/100BT transmitting output pin/ receiving input pin (positive)
B14	RXN	I	***RXN.*** 10B-T/100BT receiving input pin/ transmitting output pin (negative)
A14	RXP	I	***RXP.*** 10B-T/100BT receiving input pin/ transmitting output pin (positive)

- **VGA DVO Interface (47 PINs)**

PIN No.	Symbol	Type	Description
AA5	G_FPD[0]	O	DVO data bus
	G_TVD[0]	O	TV output data bus
AC4	G_FPD[1]	O	DVO data bus
	G_TVD[1]	O	TV output data bus
Y4	G_FPD[2]	O	DVO data bus
	G_TVD[2]	O	TV output data bus
AA6	G_FPD[3]	O	DVO data bus
	G_TVD[3]	O	TV output data bus
AB4	G_FPD[4]	O	DVO data bus
	G_TVD[4]	O	TV output data bus
AA4	G_FPD[5]	O	DVO data bus
	G_TVD[5]	O	TV output data bus
AB6	G_FPD[6]	O	DVO data bus
	G_TVD[6]	O	TV output data bus
AC5	G_FPD[7]	O	DVO data bus
	G_TVD[7]	O	TV output data bus

PIN No.	Symbol	Type	Description
V4	G_FPD[8]	O	DVO data bus
	G_TVD[8]	O	TV output data bus
	G_STRAP[1]	I	DVP2 port/Capture port select Default : Pull-down 0: DVP2 1: Captured
W6	G_FPD[9]	O	DVO Data Bus
	G_TVD[9]	O	TV output data bus
Y6	G_FPD[10]	O	DVO data bus
	G_TVD[10]	O	TV output data bus
V5	G_FPD[11]	O	DVO data bus
	G_TVD[11]	O	TV output data bus
U3	G_FPD[12]	O	DVO data bus.
	G_STRAP[2]	I	***VGA port Power-Down Enable.*** Default : Pull-High 0: Disabled 1: Enabled
U4	G_FPD[13]	O	DVO data bus.
	G_STRAP[3]	I	***DVP0 Power-Down Enable.*** Default : Pull-High 0: Disabled 1: Enabled
W5	G_FPD[14]	O	DVO data bus.
	G_STRAP[4]	I	***DVP1 Power-Down Enable*** Default: Pull-High 0: Disabled 1: Enabled
W3	G_FPD[15]	O	DVO data bus.
	G_STRAP[5]	I	***Strap Mode Select*** Default: Pull-High 0: From hardware default 1: From Flash
T3	G_FPD[21]	O	DVO data bus.

PIN No.	Symbol	Type	Description
Y1	G_FPD[18]	O	DVO data bus.
R3, V1, T3, U1, V2, Y1, Y2, W1	G_FPD[23:16]	O	DVO data bus.
AA1	G_FP1DE	O	DVO data enable
	G_TVDE	O	TV output data enable
Y3	G_FP1HS	O	DVO hsync
	G_TVHS	O	TV hsync
AA3	G_FP1VS	O	DVO vsync
	G_TVVS	O	TV vsync
	G_STRAP[6]	I	***DVP1 port/TV port select*** 0:DVP1 1:TV
U2	G_FP1CLK	O	DVO output clock
	G_TVCLKO	O	TV output clock
T4	G_TVCLKIN	I	TV input clock
AC3	G_FP1DET	I	DVO device detect
	G_TVDET	I	TV device detect
J5, K6, M5, L6, N5, M6, N6, P4	G_CAPD[7:0]	I	GPU Capture Data port.
N4	G_ENVDD	O	***Panel Power Sequence signal. "ENVDD".***
M4	G_ENBLT	O	***Panel Power Sequence signal. "Enable Backlight".***
N3	G_ENVEE	O	***Panel Power Sequence signal. "ENVEE".***
T5	G_FP2VS	O	***DVO2 Vsync.***
R2	G_FP2HS	O	***DVO2 Hsync.***
P2	G_FP2DET	I/O	***DVP2 Device Detect.***
R1	G_FP2DE	O	***DVO2 data Enabled.***
T1	G_FP2CLK	I/O	***DVP2 Output Clock.***
K5	G_CAPCLK	I	***GPU Capture Clock port.***

- **VGA DAC Interface (8 PINs)**

PIN No.	Symbol	Type	Description
M1	G_REXT	I	***RESET DAC Signal.*** An external resistor is connected between REXT and GND to determine the reference current. Default is 511 Ohm.
J1	G_IOR	O	***Analog Red.***
K1	G_IOG	O	***Analog Green.***
L1	G_IOB	O	***Analog Blue.***
P3	G_VSYNC	O	***CRT VSYNC.***
P1	G_HSYNC	O	***CRT HSYNC.***
J4	G_DDC_CLK	I/O	***VGA DDCCLK.***
K4	G_DDC_DAT	I/O	***VGA DDCDAT.***

- **VGA GPIO Interface (2 PINs)**

PIN No.	Symbol	Type	Description
H4	G_GPIO[2]	I/O	General I/O Port:clock
L4	G_GPIO[3]	I/O	General I/O Port:data
	G_STRAP[0]	I	Hardware strapping bus

- **VGA I²C Interface (4 PINs)**

PIN No.	Symbol	Type	Description
R5	G_DDC1_CLK	I/O	First DDC Clock.
R4	G_DDC1_DAT	I/O	First DDC Data.
P6	G_DDC2_CLK	I/O	Second DDC serial clock.
R6	G_DDC2_DAT	I/O	Second DDC serial data.

- **Test pins (4 PINs)**

PIN No.	Symbol	Type	Description
A1, A30, AK30, AK1	TEST	O	***TEST pins***

- **VREF Power (2 PINs)**

PIN No.	Symbol	Type	Description
AA10	VREF_DDR3DQ075	P	Reference voltage for DDR3 only. Reference voltage for inputs for SSTL interface
AE19	VREF_DDR3CA075	P	Reference voltage for DDR3 only. Reference voltage for inputs for SSTL interface

- **VGA Power & Ground (9 PINs)**

PIN No.	Symbol	Type	Description
N2	VDD_DAC09	I	0.9V digital power of DAC Power
J3	AVDD_DACR18	I	DAC Power Pin for RED Channel, 1.8V
J2	AVSS_DACR18	I	DAC Ground Pin for RED Channel
K3	AVDD_DACG18	I	DAC Power Pin for GREEN Channel, 1.8V
K2	AVSS_DACG18	I	DAC Ground Pin for GREEN Channel
L3	AVDD_DACB18	I	DAC Power Pin for BLUE Channel, 1.8V
L2	AVSS_DACB18	I	DAC Ground Pin for BLUE Channel
M3	AVDD_DACBG18	I	DAC Power Pin for Bandgap, 1.8V
M2	AVSS_DACBG18	I	DAC Ground Pin for Bandgap, 1.8V

- **PCIe Power & Ground (12 PINs)**

PIN No.	Symbol	Type	Description
C25	AVDD_PE33	I	***Analogue Power*** PCIe 3.3V Power
B23	AVDD_PE12	I	***Analogue Power*** PCIe 1.2V Power
D26	AVDD1_PE12	I	***Analogue Power*** PCIe 1.2V Power
D24	AVDD_PERX12	I	***Analogue Power*** PCIe Receiver 1.2V Power
C24	AVSS_PERX12	I	***Analogue Ground*** PCIe Receiver 1.2V Ground
B27	AVDD1_PERX12	I	***Analogue Power*** PCIe Receiver 1.2V Power
A27	AVSS1_PERX12	I	***Analogue Ground*** PCIe Receiver 1.2V Ground
A25	AVSS_PEPLL12	I	***Analogue Ground*** PCIe Analogue PLL 1.2V Ground
B25	AVDD_PEPLL12	I	***Analogue Power*** PCIe PLL 1.2V Power
D25	AVSS_PEPLL12	I	***Analogue Ground*** PCIe Analogue PLL 1.2V Ground
A23	AVSS_PE	I	PCIe Analogue Ground
C26	AVSS1_PE	I	PCIe Analogue Ground

- **SATA Power & Ground (7 PINs)**

PIN No.	Symbol	Type	Description
W30	AVSS_SATA	I	***SATA PHY***: Analogue Ground
W29	AVDD_SATA12	I	***SATA PHY***: 1.2V Analogue Power
U30	AVSS_SATARX12	I	***SATA PHY***: Receiver Analogue Ground
U29	AVDD_SATARX12	I	***SATA PHY***: Receiver 1.2V Analogue Power

PIN No.	Symbol	Type	Description
R30	AVDD_SATAPLL12	I	***SATA PHY***: PLL 1.2V Analogue Power
R29	AVSS_SATAPLL12	I	***SATA PHY***: PLL Analogue Ground
P29	AVDD_SATA33	I	***SATA PHY***: 3.3V Analogue Power

- **Ethernet Power & Ground (11 PINs)**

PIN No.	Symbol	Type	Description
B11	AVDD_EPHYPLL18	P	***E-PHY PLL 1.8V Power.***
C12	AVSS_EPHYPLL18	G	***E-PHY PLL 1.8V Ground.***
C15	AVDD_EPHYBG18	P	***E-PHY BandGap 1.8V Power.***
C14	AVSS_EPHYBG18	G	***E-PHY BandGap 1.8V Ground.***
A13	AVDD_EPHYRX18	P	***E-PHY Analog 1.8V Power for RX***
B13	AVSS_EPHYRX18	G	***E-PHY Analog 1.8V Ground for RX.***
A11	AVSS_EPHYTX18	G	***E-PHY Analog 1.8V Power for TX.***
A15	VDD_EPHY18	P	***E-PHY Digital 1.8V Power.***
B15	VSS_EPHY18	G	***E-PHY Digital 1.8 V Ground.***
A9	VDD_EPHYDL12	P	***Internal Ethernet PHY Digital Logic Cell Core 1.2V Power.***
B9	VSS_EPHYDL12	G	***Internal Ethernet PHY Digital Logic Cell Core 1.2V Ground.***

- **USB Power & Ground (24 PINs)**

PIN No.	Symbol	Type	Description
M30	AVDD_USB33	P	***Analogue Power***: USB 3.3V Power
M29	AVSS_USB33	G	***Analogue Ground***: USB 3.3V Ground

PIN No.	Symbol	Type	Description
J30	AVDD1_USB33	P	***Analogue Power***: USB 3.3V Power
J29	AVSS1_USB33	G	***Analogue Ground***: USB 3.3V Ground
F30	AVDD2_USB33	P	***Analogue Power***: USB 3.3V Power
F29	AVSS2_USB33	G	***Analogue Ground***: USB 3.3V Ground
C30	AVDD3_USB33	P	***Analogue Power***: USB 3.3V Power
C29	AVSS3_USB33	G	***Analogue Ground***: USB 3.3V Ground
J28	AVDD_USBBAS33	I	***Analogue Power***: USB Base Voltage 3.3V Power
N28	AVSS_USBBAS33	G	***Analogue Ground***: USB Base Voltage 3.3V Ground
C28	AVDD2_USBBAS33	I	***Analogue Power***: USB Base Voltage 3.3V Power
G28	AVSS2_USBBAS33	G	***Analogue Ground***: USB Base Voltage 3.3V Ground
L28	AVDD_USB12	P	***Analogue Power***: USB 1.2V Power
H28	AVDD1_USB12	P	***Analogue Power***: USB 1.2V Power
E28	AVDD2_USB12	P	***Analogue Power***: USB 1.2V Power
B28	AVDD3_USB12	P	***Analogue Power***: USB 1.2V Power
K30	AVDD_USBPLL12	P	***USB PLL Power***
K29	AVSS_USBPLL12	G	***USB PLL Ground***

PIN No.	Symbol	Type	Description
G30	AVDD1_USBPLL12	P	***USB PLL Power***
G29	AVSS1_USBPLL12	G	***USB PLL Ground***
D30	AVDD2_USBPLL12	P	***USB PLL Power***
D29	AVSS2_USBPLL12	G	***USB PLL Ground***
A29	AVDD3_USBPLL12	P	***USB PLL Power***
A28	AVSS3_USBPLL12	G	***USB PLL Ground***

- **ADC Power & Ground (14 PINs)**

PIN No.	Symbol	Type	Description
E18	AVDD_VREFP_ADC33	P	***Analogue reference 3.3V Power for ADC.***
D18	AVSS_ADCVREFN33	G	***Analogue reference 3.3V Ground for ADC.***
E17	AVDD_ADC33	P	***Analogue 3.3V Power for ADC.***
D17	AVSS_ADC33	G	***Analogue 3.3V Ground for ADC.***
F16	VDD_ADC33	P	***Digital 3.3V Power for ADC.***
E16	VSS_ADC33	G	***Digital 3.3V Ground for ADC.***
F21	AVDD_TEMP18	P	***Analog 1.8V Power for Temp. Sensor.***
E21	AVSS_TEMP18	G	***Analog 1.8V Ground for Temp. Sensor.***
D21	VDD_TEMP18	P	***Digital 1.8V Power for Temp. Sensor.***
C21	VSS_TEMP18	G	***Digital 1.8V Ground for Temp. Sensor.***
C16	AVDD_PLL18	P	***1.8V PLL Power.***
C17	AVSS_PLL18	G	***1.8V PLL Ground.***
C18	AVDD_PLL18	P	***1.8V PLL Power.***
C19	AVSS_PLL18	G	***1.8V PLL Ground.***

- **Battery Power & Ground (2 PINs)**

PIN No.	Symbol	Type	Description
D7	VDD_BAT	P	Battery power for RTC
A8	VSS_BAT	G	Battery ground for RTC

- **0.9V Power (12 PINs)**

PIN No.	Symbol	Type	Description
T10, T12, U6, U13, U14, V14, Y14, Y15, AA15, AD6, AE9, AE11	VDD09 (12 PINs)	P	***Core Power for Chip.***

- **1.2V Power (16 PINs)**

PIN No.	Symbol	Type	Description
F23, G25, K15, M17, R25, T18, T20, T21	VDD12 (8 PINs)	P	***1.2V Power.***
A16, A18, A21, C23	VDD_DIF12 (4 PINs)	P	***Differential PAD 1.2V Power.***
B16, B18, B21, C22	VSS_DIF12 (4 PINs)	G	***Differential PAD 1.2V Ground.***

- **1.5V Power (18 PINs)**

PIN No.	Symbol	Type	Description
AA11, AD2, AD3, AE7, AE10, AE12, AE16, AE17, AE20, AF4, AG2, AG8, AG14, AH5, AH16, AH18, AJ12, AK6	VDD15 (18 PINs)	P	***1.5V Power.***

- **1.8V POWER (22 PINs)**

PIN No.	Symbol	Type	Description
T11, T13, V3, V6, V15, W4, AB3, AC6	VDD18 (8 PINs)	P	***1.8V Power.***
K17, L16, N17, P15	VDD_SB18 (4 PINs)	P	***South Bridge 1.8V Power.***
AA14	AVDD_DDRPHYPLL18	P	***Analog Power for DDR3 PHY PLL.***
AA13	AVSS_DDRPHYPLL18	G	***Analog Ground for DDR3 PHY PLL.***
P10	AVDD_NBVGAPLL18	P	***Analog Power for VGA1 & VGA2 PLL.***
R10	AVSS_NBVGAPLL18	G	***Analog Ground for VGA1 & VGA2 PLL.***
AC2	AVDD_NBDDRPLL18	P	***Analog Power for DRAM PLL..***
AB2	AVSS_NBDDRPLL18	G	***Analog Ground for DRAM PLL..***
AC1	AVDD_NBCPUPLL18	P	***Analog Power for CPU PLL.***
AB1	AVSS_NBCPUPLL18	G	***Analog Ground for CPU PLL.***
U10	AVDD_NBTEMP18	P	***Analog Power for Temp. Sensor.***
V10	AVSS_NBTEMP18	G	***Analog Ground for Temp. Sensor.***

- **3.3V Power (9 PINs)**

PIN No.	Symbol	Type	Description
F24, G3, J6, K18, P18, P20, P25, R20, T6	VDD33 (9 PINs)	P	***3.3V Power.***

- **Digital Ground (157 PINs)**

PIN No.	Symbol	Type	Description
B2, B5, B8, C10, C20, E2, E5, E7, E10, E13, E15, E22, F25, F27, G6, H1, H2, H5, H26, K27, L5, L17, L18, L19, L20, L25, M11, M12, M13, M15, M16, M18, M19, M20, M27, N1, N10, N12, N13, N14, N15, N16, N18, N19, N20, N29, P5, P11, P12, P13, P14, P16, P17, P19, P26, P28, R11, R12, R13, R14, R15, R16, R17, R18, R19, R21, T2, T14, T15, T16, T17, T19, T28, U5, U11, U12, U15, U16, U17, U18, U19, V11, V12, V13,	VSS (157 PINs)	G	***Digital Ground.***

PIN No.	Symbol	Type	Description
V16, V17, V18, V19, V25, V28, W2, W10, W11, W12, W13, W14, W15, W16, W17, W18, W19, Y5, Y10, Y11, Y12, Y13, Y16, Y17, Y18, Y19, Y30, AA2, AA16, AA17, AA18, AA19, AA20, AA21, AA26, AB5, AB28, AC30, AD1, AD4, AD5, AD29, AE8, AE14, AE18, AE27, AF2, AF6, AF9, AF11, AF19, AF21, AF25, AG4, AG10, AG12, AG17, AH2, AH7, AH11, AH15, AH19, AH27, AH29, AJ5, AJ8, AJ13, AJ17, AJ22, AJ25, AK3, AK10, AK20			

- **NC Pin (4 PINs)**

PIN No.	Symbol	Type	Description
N11, D16, B10, A10	NC	NC	***NC.***

5.3. PIN Capacitance Description

5.3.1. North-Bridge

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	1.94304	2.05082	2.08563	pF
C_{BID}	3.3V Bi-directional Capacitance	2.18057(max loading=40)	2.21818(max loading=40)	2.2269(max loading=40)	pF

5.3.2. VGA

Symbol	Parameter	Min.	Max.	Unit
C_{BID}	3.3V Bi-directional Capacitance	2(max loading=40)	2.5(max loading=40)	pF

5.3.3. South-Bridge

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{IN}	3.3V Input Capacitance	3.144	3.143	3.216	pF
C_{BID}	3.3V Bi-directional Capacitance	3.179	3.116	3.099	pF

5.4. PIN Pull-up / Pull-down Description

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
PWRGOOD	I	3.3V	--	--	--	Y	--	--	
CLK25MOUT	O	3.3V	SF0-44h	--	--	--	--	SF0-44h	
CLK24MOUT	O	3.3V	SF0-44h	--	--	--	--	SF0-44h	
XOUT_14318	O	1.8V	--	--	--	--	--	--	
XIN_14318	I	1.8V	--	--	--	--	--	--	
SPEAKER	O	3.3V	8mA	--	Y	--	--	S	
PCIRST#	O	1.8V	SF0-48h	--	--	--	--	--	
UD_DP	I/O	3.3V	D1060_config-40h[5:4]	--	--	D1060_config-40h[1]	Y	D1060_config-40h[2]	
UD_DM	I/O	3.3V	D1060_current-40h[5:4]	--	--	D1060_current-40h[1]	Y	D1060_current-40h[2]	
SD[15:0]	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
IRQ[15:14],	I	3.3V	--	Y	--	Y	Y	--	
IRQ[12:9],	I	3.3V	--	Y	--	Y	Y	--	
IRQ[7:3]	I	3.3V	--	Y	--	Y	Y	--	
DRQ[7:5]	I	3.3V	--	--	Y	Y	Y	--	
DRQ[3:0]	I	3.3V	--	--	Y	Y	Y	--	
ISA_SA[31:24]	I/O	3.3V	SF0-48h[21:20]	--	--	SF1-40h[18]	Y	SF1-40h[2]	
SA[19:0]	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
DACK#[7:5],	O	3.3V	SF0-44h	Y	--	--	Y	S	
DACK#[3:0]	O	3.3V	SF0-44h	Y	--	--	Y	S	
LA[23:17]	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
IOCHCK#	I	3.3V	--	Y	--	Y	Y	--	
IOCHRDY	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
IOCS16#	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
SBHE#	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
SMEMR#	O	3.3V	SF0-44h	Y	--	--	Y	S	
SMEMW#	O	3.3V	SF0-44h	Y	--	--	Y	S	
MEMR#	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
MEMW#	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
MEMCS16#	I/O	3.3V	SF0-44h	Y	--	Y	Y	S	
0WS#	I	3.3V	--	Y	--	Y	Y	--	
IOR#	O	3.3V	SF0-44h	Y	--	--	Y	S	
IOW#	O	3.3V	SF0-44h	Y	--	--	Y	S	
REFRESH#	O	3.3V	SF0-44h	Y	--	Y	Y	S	
AEN	O	3.3V	SF0-44h	--	Y	--	Y	S	
RST_DRV	O	3.3V	SF0-44h	--	Y	--	Y	F	
SYSCLK	O	3.3V	SF0-44h	Y	--	Y	Y	SF0-44h	
TC	O	3.3V	SF0-44h	--	Y	--	Y	S	
BALE	O	3.3V	SF0-44h	--	Y	--	Y	S	
OSC14318	O	3.3V	SF0-44h	--	--	--	Y	SF0-44h	
ROM_CS#	O	1.8V	8mA	--	--	--	--	S	
GPCS0#	O	3.3V	SF0-44h	Y	--	--	Y	F	
GPCS1#	O	3.3V	SF0-44h	Y	--	--	Y	F	
SPI_CS#	O	1.8V	8mA	--	--	--	--	--	
SPI_CLK	O	1.8V	8mA	--	--	--	--	--	
SPI_DO	O	1.8V	8mA	--	--	--	--	--	
SPI_DI	I	1.8V	--	--	--	--	--	--	
E_SPI_DI	I	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
E_SPI_DO	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
E_SPI_CLK	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
E_SPI_CS#	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
EXTSYSFAILIN#	I	3.3V	--	--	Y	Y	Y	--	
EXT_SWITCH_FAIL#	I	3.3V	--	Y	--	Y	Y	--	
EXT_GPCS#	I	3.3V	--	Y	--	Y	Y	--	
SYSFAILOUT#	O	3.3V	12mA	--	--	--	Y	S	
KBCLK/ KBRST#	I/O	3.3V	16mA	Y	--	Y	Y	S	
KBDAT/ A20GATE#	I/O	3.3V	16mA	Y	--	Y	Y	S	
MSCLK	I/O	3.3V	16mA	Y	--	Y	Y	S	
MSDAT	I/O	3.3V	16mA	Y	--	Y	Y	S	
TDO	O	3.3V	6mA	--	--	Y	N	S	
TMS	I	3.3V	--	--	--	Y	N	S	
TCK	I	3.3V	--	--	--	Y	N	S	
TDI	I	3.3V	--	--	--	Y	N	S	
GPIO_P0[7:0]	I/O	3.3V	SF0-48h [17:16]	SF1-44h[0]	SF1-44h[1]	SF1-40h [16]	Y	SF1-40h [0]	
GPIO_P1[7:0]	I/O	3.3V	SF0-48h [19:18]	SF1-44h[2]	SF1-44h[3]	SF1-40h [17]	Y	SF1-40h [1]	
GPIO_P2[7:0]	I/O	3.3V	SF0-48h [21:20]	SF1-44h[4]	SF1-44h[5]	SF1-40h [18]	Y	SF1-40h [2]	
GPIO_P3[7:0]	I/O	3.3V	SF0-48h [27:22]	SF1-44h[6]	SF1-44h[7]	SF1-40h [19]	Y	SF1-40h [3]	
GPIO_P4[7:0]	I/O	3.3V	SF0-48h [29:28]	SF1-44h[8]	SF1-44h[9]	SF1-40h [20]	Y	SF1-40h [4]	
GPIO_P5[7:0]	I/O	3.3V	SF1-48h [1:0]	SF1-44h[10]	SF1-44h[11]	SF1-40h [21]	Y	SF1-40h [5]	
GPIO_P6[7:0]	I/O	3.3V	SF1-48h [3:2]	SF1-44h[12]	SF1-44h[13]	SF1-40h [22]	Y	SF1-40h [6]	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
GPIO_P7[7:0]	I/O	3.3V	SF1-48h [5:4]	SF1-44h[14]	SF1-44h[15]	SF1-40h [23]	Y	SF1-40h [7]	
GPIO_P8[7:0]	I/O	3.3V	SF1-48h [7:6]	SF1-44h[16]	SF1-44h[17]	SF1-40h [24]	Y	SF1-40h [8]	
GPIO_P9[7:0]	I/O	3.3V	SF1-48h [9:8]	SF1-44h[18]	SF1-44h[19]	SF1-40h [27:25]	Y	SF1-40h [11:9]	
GPIO_PA[7:0]	I/O	3.3V	SF1-48h [11:10]	SF1-44h[20]	SF1-44h[21]	SF1-40h [29:28]	Y	SF1-40h [13:12]	
8051A_GPIO_P0[7:0]	I/O	3.3V	SF0-48h [17:16]	SF1-44h[0]	SF1-44h[1]	SF1-40h [16]	Y	SF1-40h [0]	
8051A_GPIO_P1[7:0]	I/O	3.3V	SF0-48h [19:18]	SF1-44h[2]	SF1-44h[3]	SF1-40h [17]	Y	SF1-40h [1]	
8051A_GPIO_P2[7:0]	I/O	3.3V	SF0-48h [21:20]	SF1-44h[4]	SF1-44h[5]	SF1-40h [18]	Y	SF1-40h [2]	
8051A_GPIO_P3[7:0]	I/O	3.3V	SF0-48h [27:22]	SF1-44h[6]	SF1-44h[7]	SF1-40h [19]	Y	SF1-40h [3]	
8051A_GPIO_P4[7:0]	I/O	3.3V	SF0-48h [29:28]	SF1-44h[8]	SF1-44h[9]	SF1-40h [20]	Y	SF1-40h [4]	
8051B_GPIO_P0[7:0]	I/O	3.3V	SF0-48h [17:16]	SF1-44h[0]	SF1-44h[1]	SF1-40h [16]	Y	SF1-40h [0]	
8051B_GPIO_P1[7:0]	I/O	3.3V	SF0-48h [19:18]	SF1-44h[2]	SF1-44h[3]	SF1-40h [17]	Y	SF1-40h [1]	
8051B_GPIO_P2[7:0]	I/O	3.3V	SF0-48h [21:20]	SF1-44h[4]	SF1-44h[5]	SF1-40h [18]	Y	SF1-40h [2]	
8051B_GPIO_P3[5:0]	I/O	3.3V	SF0-48h [25:22]	SF1-44h[6]	SF1-44h[7]	SF1-40h [19]	Y	SF1-40h [3]	
8051B_GPIO_P4[7:0]	I/O	3.3V	SF0-48h [29:28]	SF1-44h[8]	SF1-44h[9]	SF1-40h [20]	Y	SF1-40h [4]	
8051B_GPIO_P5[7:0]	I/O	3.3V	SF1-48h [1:0]	SF1-44h[10	SF1-44h[11]	SF1-40h [21]	Y	SF1-40h [5]	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
				]					
8051B_GPIO_P6[7:0]	I/O	3.3V	SF1-48h [3:2]	SF1-44h[12]	SF1-44h[13]	SF1-40h [22]	Y	SF1-40h [6]	
8051B_GPIO_P7[7:0]	I/O	3.3V	SF1-48h [5:4]	SF1-44h[14]	SF1-44h[15]	SF1-40h [23]	Y	SF1-40h [7]	
8051B_GPIO_P8[7:0]	I/O	3.3V	SF1-48h [7:6]	SF1-44h[16]	SF1-44h[17]	SF1-40h [24]	Y	SF1-40h [8]	
8051B_GPIO_P9[7:0]	I/O	3.3V	SF1-48h [9:8]	SF1-44h[18]	SF1-44h[19]	SF1-40h [27:25]	Y	SF1-40h [11:9]	
8051B_SOUT1	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
8051B_SIN1	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
8051B_SOUT2	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
8051B_SIN2	I	3.3V	SF0-48h [25:24]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
8051B_TXDEN1	I/O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
8051B_TXDEN2	I/O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
MC0[4,5,3:0]	I/O	3.3V	SF0-48h [17:16]	Note 1	Note 1	SF1-40h [16]	Y	SF1-40h [0]	
MC1[4,5,3:0]	I/O	3.3V	SF0-48h [19:18]	Note 1	Note 1	SF1-40h [17]	Y	SF1-40h [1]	
MC2[4,5,3:0]	I/O	3.3V	SF0-48h [21:20]	Note 1	Note 1	SF1-40h [18]	Y	SF1-40h [2]	
MC3[5:0]	I/O	3.3V	SF0-48h [21:16]	Note 1	Note 1	SF1-40h [18:16]	Y	SF1-40h [2:0]	
MC4[4,5,3:0]	I/O	3.3V	SF0-48h	Note	Note	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[29:28]	1	1	[20]		[4]	
MC5[4,5,3:0]	I/O	3.3V	SF1-48h [1:0]	Note 1	Note 1	SF1-40h [21]	Y	SF1-40h [5]	
MC6[4,5,3:0]	I/O	3.3V	SF1-48h [3:2]	Note 1	Note 1	SF1-40h [22]	Y	SF1-40h [6]	
MC7[7:0]	I/O	3.3V	Note 2	Note 1	Note 1	SF1-40h [22:20]	Y	SF1-40h [6:4]	
MC8[4,5,3:0]	I/O	3.3V	SF1-48h [5:4]	Note 1	Note 1	SF1-40h [23]	Y	SF1-40h [7]	
MC9[4,5,3:0]	I/O	3.3V	SF1-48h [7:6]	Note 1	Note 1	SF1-40h [24]	Y	SF1-40h [8]	
MCA[4,5,3:0]	I/O	3.3V	SF1-48h [9:8]	Note 1	Note 1	SF1-40h [26:25]	Y	SF1-40h [10:9]	
MCB[5:0]	I/O	3.3V	SF1-48h [9:4]	Note 1	Note 1	Note 3	Y	Note 3	
FD_SPI1_DI	I	3.3V	SF0-48h [23:22]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
FD_SPI1_DO	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
FD_SPI1_CLK	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
FD_SPI1_CS#	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
FD_SPI2_DI	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
FD_SPI2_DO	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
FD_SPI2_CLK	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
FD_SPI2_CS#	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
CTS1#	I	3.3V	SF0-48h [29:28]	Y	--	SF1-40h [20]	Y	SF1-40h [4]	
RTS1#	O	3.3V	SF0-48h	--	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[29:28]			[20]		[4]	
DTR1#	O	3.3V	SF0-48h [29:28]	--	--	SF1-40h [20]	Y	SF1-40h [4]	
DSR1#	I	3.3V	SF0-48h [29:28]	Y	--	SF1-40h [20]	Y	SF1-40h [4]	
DCD1#	I	3.3V	SF0-48h [29:28]	Y	--	SF1-40h [20]	Y	SF1-40h [4]	
SIN1	I	3.3V	SF0-48h [29:28]	Y	--	SF1-40h [20]	Y	SF1-40h [4]	
RI1#	I	3.3V	SF0-48h [29:28]	Y	--	SF1-40h [20]	Y	SF1-40h [4]	
SOUT1	O	3.3V	SF0-48h [29:28]	--	--	SF1-40h [20]	Y	SF1-40h [4]	
CTS2#	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
RTS2#	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
DTR2#	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
DSR2#	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
DCD2#	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
SIN2	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
RI2#	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
SOUT2	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
CTS3#	I	3.3V	SF1-48h [3:2]	Y	--	SF1-40h [22]	Y	SF1-40h [6]	
RTS3#	O	3.3V	SF1-48h [3:2]	--	--	SF1-40h [22]	Y	SF1-40h [6]	
DTR3#	O	3.3V	SF1-48h	--	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[3:2]			[22]		[6]	
DSR3#	I	3.3V	SF1-48h [3:2]	Y	--	SF1-40h [22]	Y	SF1-40h [6]	
DCD3#	I	3.3V	SF1-48h [3:2]	Y	--	SF1-40h [22]	Y	SF1-40h [6]	
SIN3	I	3.3V	SF1-48h [3:2]	Y	--	SF1-40h [22]	Y	SF1-40h [6]	
RI3#	I	3.3V	SF1-48h [3:2]	Y	--	SF1-40h [22]	Y	SF1-40h [6]	
SOUT3	O	3.3V	SF1-48h [3:2]	--	--	SF1-40h [22]	Y	SF1-40h [6]	
CTS4#	I	3.3V	SF1-48h [5:4]	Y	--	SF1-40h [23]	Y	SF1-40h [7]	
RTS4#	O	3.3V	SF1-48h [5:4]	--	--	SF1-40h [23]	Y	SF1-40h [7]	
DTR4#	O	3.3V	SF1-48h [5:4]	--	--	SF1-40h [23]	Y	SF1-40h [7]	
DSR4#	I	3.3V	SF1-48h [5:4]	Y	--	SF1-40h [23]	Y	SF1-40h [7]	
DCD4#	I	3.3V	SF1-48h [5:4]	Y	--	SF1-40h [23]	Y	SF1-40h [7]	
SIN4	I	3.3V	SF1-48h [5:4]	Y	--	SF1-40h [23]	Y	SF1-40h [7]	
RI4#	I	3.3V	SF1-48h [5:4]	Y	--	SF1-40h [23]	Y	SF1-40h [7]	
SOUT4	O	3.3V	SF1-48h [5:4]	--	--	SF1-40h [23]	Y	SF1-40h [7]	
CTS5#	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
RTS5#	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
DTR5#	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
DSR5#	I	3.3V	SF0-48h	Y	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[17:16]			[16]		[0]	
DCD5#	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
RI5#	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
SIN5	I	3.3V	SF0-48h [17:16]	Y	--	SF1-40h [16]	Y	SF1-40h [0]	
SOUT5	O	3.3V	SF0-48h [17:16]	--	--	SF1-40h [16]	Y	SF1-40h [0]	
CTS6#	I	3.3V	SF0-48h [19:18]	Y	--	SF1-40h [17]	Y	SF1-40h [1]	
RTS6#	O	3.3V	SF0-48h [19:18]	--	--	SF1-40h [17]	Y	SF1-40h [1]	
DTR6#	O	3.3V	SF0-48h [19:18]	--	--	SF1-40h [17]	Y	SF1-40h [1]	
DSR6#	I	3.3V	SF0-48h [19:18]	Y	--	SF1-40h [17]	Y	SF1-40h [1]	
DCD6#	I	3.3V	SF0-48h [19:18]	Y	--	SF1-40h [17]	Y	SF1-40h [1]	
RI6#	I	3.3V	SF0-48h [19:18]	Y	--	SF1-40h [17]	Y	SF1-40h [1]	
SIN6	I	3.3V	SF0-48h [19:18]	Y	--	SF1-40h [17]	Y	SF1-40h [1]	
SOUT6	O	3.3V	SF0-48h [19:18]	--	--	SF1-40h [17]	Y	SF1-40h [1]	
CTS7#	I	3.3V	SF0-48h [21:20]	Y	--	SF1-40h [18]	Y	SF1-40h [2]	
RTS7#	O	3.3V	SF0-48h [21:20]	--	--	SF1-40h [18]	Y	SF1-40h [2]	
DTR7#	O	3.3V	SF0-48h [21:20]	--	--	SF1-40h [18]	Y	SF1-40h [2]	
DSR7#	I	3.3V	SF0-48h [21:20]	Y	--	SF1-40h [18]	Y	SF1-40h [2]	
DCD7#	I	3.3V	SF0-48h	Y	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[21:20]			[18]		[2]	
RI7#	I	3.3V	SF0-48h [21:20]	Y	--	SF1-40h [18]	Y	SF1-40h [2]	
SIN7	I	3.3V	SF0-48h [21:20]	Y	--	SF1-40h [18]	Y	SF1-40h [2]	
SOUT7	O	3.3V	SF0-48h [21:20]	--	--	SF1-40h [18]	Y	SF1-40h [2]	
CTS8#	I	3.3V	SF0-48h [27:26]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
RTS8#	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
DTR8#	O	3.3V	SF0-48h [25:24]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
DSR8#	I	3.3V	SF0-48h [27:26]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
DCD8#	I/O	3.3V	SF0-48h [23:22]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
RI8#	I/O	3.3V	SF0-48h [23:22]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
SIN8	I/O	3.3V	SF0-48h [25:24]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
SOUT8	O	3.3V	SF0-48h [23:22]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
CTS9#	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
RTS9#	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	
DTR9#	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	
DSR9#	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
DCD9#	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
RI9#	I	3.3V	SF1-48h	Y	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[7:6]			[24]		[8]	
SIN9	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
SOUT9	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	
COM3_TXDEN	O	3.3V	SF0-48h [27:26]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
COM4_TXDEN	O	3.3V	SF0-48h [27:26]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
RTC_RD#	O	3.3V	SF0-48h [27:26]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
RTC_WR#	O	3.3V	SF0-48h [25:24]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
RTC_IRQ8#	I	3.3V	SF0-48h [25:24]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
RTC_AS	O	3.3V	SF0-48h [27:26]	--	--	SF1-40h [19]	Y	SF1-40h [3]	
RTC_PS	I	3.3V	--	--	--	--	--	--	
RTC_XOUT	O	3.3V	--	--	--	--	--	--	
RTC_XI	I	3.3V	--	--	--	--	--	--	
I2C_SDA	I/O	3.3V	SF0-48h [25:24]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
I2C_SCL	I/O	3.3V	SF0-48h [25:24]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
I2C1_SDA	I/O	3.3V	SF0-48h [27:26]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
I2C1_SCL	I/O	3.3V	SF0-48h [27:26]	Y	--	SF1-40h [19]	Y	SF1-40h [3]	
PWM_GATE	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM_OUT	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM_CLK	I	3.3V	SF1-48h	Y	--	SF1-40h	Y	SF1-40h	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
			[1:0]			[21]		[5]	
PWM1_GATE	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM1_OUT	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM1_CLK	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM2_GATE	I	3.3V	SF1-48h [11:10]	--	--	SF1-40h [28]	Y	SF1-40h [12]	
PWM2_OUT	O	3.3V	SF1-48h [1:0]	--	--	SF1-40h [21]	Y	SF1-40h [5]	
PWM2_CLK	I	3.3V	SF1-48h [1:0]	Y	--	SF1-40h [21]	Y	SF1-40h [5]	
IDE_PDD[15:0]	I/O	3.3V	IDE_con fig-80h[2:0]	--	Y	--	Y	--	
IDE_PA[2:0]	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
IDE_PCS1#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
IDE_PCS0#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
IDE_PIOW#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
IDE_PINT	I	3.3V	IDE_con fig-80h[2:0]	--	Y	--	Y	--	
IDE_PIOR#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
IDE_PDRQ	I	3.3V	IDE_con fig-80h[2:0]	--	Y	--	Y	--	
IDE_PIORDY	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
IDE_PDACK#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
IDE_PCBLID#	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
IDE_PRST#	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
SD_DATA[3:0]	I/O	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD_WP	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD_CD	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD_CLK	O	3.3V	IDE_con fig-80h[2:0]	--	Y	--	Y	--	
SD_CMD	I/O	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD_ACTIVE	O	3.3V	IDE_con fig-80h[2:0]]	--	--	--	Y	--	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
SD1_DATA[3:0]	I/O	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD1_WP	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD1_CD	I	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD1_CLK	O	3.3V	IDE_con fig-80h[2:0]	--	Y	--	Y	--	
SD1_CMD	I/O	3.3V	IDE_con fig-80h[2:0]	Y	--	--	Y	--	
SD1_ACTIVE	O	3.3V	IDE_con fig-80h[2:0]	--	--	--	Y	--	
MTBF	O	3.3V	SF1-48h [9:8]	--	--	SF1-40h [27]	Y	SF1-40h [11]	
WDT_RSTB	O	3.3V	SF1-48h [9:8]	--	--	SF1-40h [27]	Y	SF1-40h [11]	
PD[7:0]	I/O	3.3V	SF1-48h [9:8]	--	--	SF1-40h [27:25]	Y	SF1-40h [11:9]	
AFD#	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	
ACK#	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
BUSY	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
ERR#	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
INIT#	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
SLCIN	O	3.3V	SF1-48h [7:6]	--	--	SF1-40h [24]	Y	SF1-40h [8]	
SLCT	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
PE	I	3.3V	SF1-48h [7:6]	Y	--	SF1-40h [24]	Y	SF1-40h [8]	
STB#	O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [29]	Y	SF1-40h [13]	
TX_DEN1	O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [29]	Y	SF1-40h [13]	
TX_DEN2	O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [29]	Y	SF1-40h [13]	
H_BCLK	O	3.3V	8mA	--	Y	Y	Y	Y	
H_SYNC	O	3.3V	8mA	--	Y	Y	Y	Y	
H_SDO	O	3.3V	8mA	--	Y	Y	Y	Y	
H_SDI	I/O	3.3V	8mA	--	Y	Y	Y	Y	
H_RST#	O	3.3V	8mA	Y	--	Y	Y	Y	
GSF_CH0	I/O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [28]	Y	SF1-40h [12]	
GSF_CH1	I/O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [28]	Y	SF1-40h [12]	
GSF_CH2	I/O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [28]	Y	SF1-40h [12]	
GSF_CLK	O	3.3V	SF1-48h [11:10]	--	--	SF1-40h [28]	Y	SF1-40h [12]	
LINK/ACTIVE	O	3.3V	8mA	--	--	--	--	S	
DUPLEX	O	3.3V	8mA	--	--	--	--	S	
MDC	O	3.3V	6mA	--	--	--	--	S	
MDIO	I/O	3.3V	6mA	Y	--	--	--	--	
COL	I	3.3V	--	--	--	Y	--	--	
RXC	I	3.3V	--	--	--	Y	--	--	
RXDV	I	3.3V	--	--	--	Y	--	--	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
TXC	I	3.3V	--	--	--	Y	--	--	
TXEN	O	3.3V	6mA	--	--	--	--	S	
G_FPD[23:16]	I/O	1.8V	8mA	--	--	--	--	--	
G_FPD[15:12]	I/O	1.8V	8mA	Y	--	--	--	--	
G_FPD[11:10]	I/O	1.8V	8mA	--	--	--	--	--	
G_FPD[9]	I/O	1.8V	8mA	--	Y	--	--	--	
G_FPD[7:8]	I/O	1.8V	8mA	--	--	--	--	--	
G_FPD[6]	I/O	1.8V	8mA	--	Y	--	--	--	
G_FPD[5:0]	I/O	1.8V	8mA	--	--	--	--	--	
G_FP1DE	I/O	1.8V	8mA	--	--	--	--	--	
G_FP1DET	I/O	1.8V	8mA	--	--	--	--	--	
G_FP1HS	I/O	1.8V	8mA	--	--	--	--	--	
G_FP1VS	I/O	1.8V	8mA	--	--	--	--	--	
G_FP1CLK	I/O	1.8V	8mA	--	--	--	--	--	
G_FP2DE	I/O	1.8V	8mA	--	--	--	--	--	
G_FP2DET	I/O	1.8V	8mA	--	--	--	--	--	
G_FP2HS	I/O	1.8V	8mA	--	--	--	--	--	
G_FP2VS	I/O	1.8V	8mA	--	--	--	--	--	
G_FP2CLK	I/O	1.8V	8mA						
G_TVCLKIN	I	3.3V	--	--	--	--	--	--	
G_ENVDD	I/O	3.3V	8mA	--	Y	--	--	--	
G_ENBLT	I/O	3.3V	8mA	--	Y	--	--	--	
G_ENVEE	I/O	3.3V	8mA	--	Y	--	--	--	
G_VSYNC	O	1.8V	8mA	--	--	--	--	--	
G_HSYNC	O	1.8V	8mA	--	--	--	--	--	
G_GPIO[3:2]	I/O	3.3V	8mA	Y	--	--	--	--	
G_DDC_CLK	I/O	3.3V	8mA	Y	--	--	--	--	
G_DDC_DAT	I/O	3.3V	8mA	Y	--	--	--	--	
G_DDC1_CLK	I/O	3.3V	8mA	Y	--	--	--	--	
G_DDC1_DAT	I/O	3.3V	8mA	Y	--	--	--	--	

PIN Name	Type	Volt-age	Driving Current	Pull-Up	Pull-Down	Schmitt Trigger	5V I/O Tolerant	Slew Rate	Descrip-tion
G_DDC2_CLK	I/O	3.3V	8mA	Y	--	--	--	--	
G_DDC2_DAT	I/O	3.3V	8mA	Y	--	--	--	--	

Definition:

--: Not need to specify

Y: Yes

F: Fast

S: Slow

The pull-up/pull-down resistance is 75KΩ

Note 1: MC Port State Control Register (MCPSCR) 44h.

Note 2: MC7[5:2] is programmable through SF1-48h[3:0]; MC7[1:0] is programmable through SF0-48h[29:28].

Note 3: MCB[5:4]: Schmitt Trigger value is programmable through SF0-48h[27:26] and the Slew Rate value is programmable through SF1-40h[11:10]; MCB[3:0]: programmable through SF0-48h[24:23] and the Slew Rate value is programmable through SF1-40h[8:7].

Note 4: SB F0/1 xh[y]: South Bridge Function 0/1, offest xh[bit y].

Note 5: The capability of these I/O pins withstand a voltage up to 5.5V.

5.5. PIN Function only reset by PWRGOOD

These pin functions are only reset by PWRGOOD

1. GPIO_0~A Direction register
2. GPIO_0~A Data register
3. South Configuration Register 40h
4. South Function 0 Configuration Register 60h~6Fh
5. South Function 1 Configuration Register 60h~6Ch
6. South Function 1 Configuration Register 6Eh~6Fh

6. System Address Map

The SoC supports 4 Gbytes of addressable memory space and 64 Kbytes of addressable I/O space. In order to be compatible with PC/AT system, the lower 1 Mbyte of this addressable memory is divided into regions which can be individually controlled with programmable attributes such as disable, read/write, write only, or read only (see Chapter 12, Register Description section for details on attribute programming).

6.1. Memory Address Ranges

Figure 6-1 represents SoC memory address map. It shows the main memory regions defined and supported by the SoC. At the highest level, the address space is divided into two main conceptual regions. One is the 0–1-Mbyte DOS compatibility region and the other is 1-Mbyte to 4-Gbyte extended memory region. The SoC supports several main memory sizes (**Figure 6-1**). The main memory type and size in the system will be auto-detected by the system BIOS.

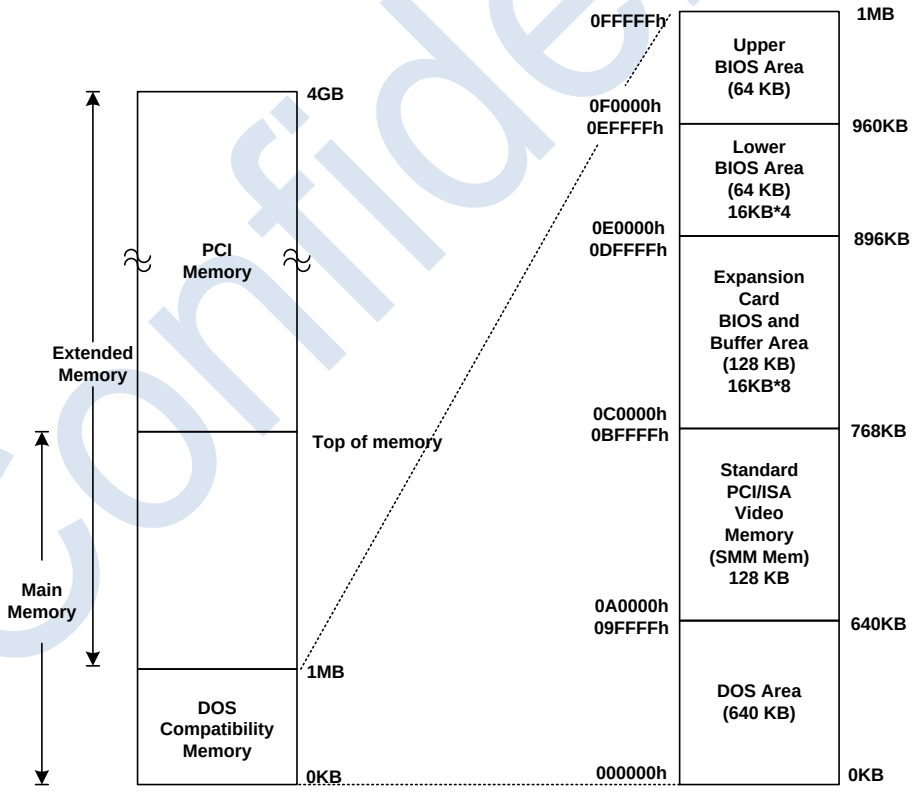


Figure 6-1. Memory Address Map

6.1.1. Dos Compatibility Region

The first region of memory is called the Dos Compatibility Region because it is defined for early PC. This area is divided into the following address regions:

- 0–640-Kbyte DOS Area
- 640–768-Kbyte Video Buffer Area
- 768–896-Kbyte in 16-Kbyte sections (total of 8 sections) - Expansion Area
- 896–960-Kbyte in 16-Kbyte sections (total of 4 sections) - Extended System BIOS Area
- 960-Kbyte–1-Mbyte Memory (BIOS Area) - System BIOS Area

From 640 Kbytes – 1 Mbyte: it can be divided into fourteen ranges which can be enabled or disabled independently for both read and write. These regions can also be mapped to either main DRAM or PCI by system BIOS. (See A/B Page and SMM Range Register and Shadow RAM Register in Chapter 12.)

DOS Area (00000–9FFFFh)

The DOS area (00000h – 9FFFFh) is 640 Kbytes in size. It is always mapped to the main memory controlled by the SoC.

Video Buffer Area (A0000–BFFFFh)

The 128-Kbyte graphics adapter memory region is normally mapped to a video device on the PCI bus (typically VGA controller). This area is controlled by the A/B Page and SMM Range Register. It can be mapped to either main DRAM or PCI for both read and write command.

ISA Expansion Area (C0000–DFFFFh)

This 128-Kbyte ISA Expansion region is divided into eight 16-Kbyte segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the PCI bridge to ISA space. Memory that is disabled is not remapped.

Extended System BIOS Area (E0000–EFFFFh)

This 64-Kbyte area is divided into four 16-Kbyte segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to PCI. Typically, this area is used for RAM or ROM. Memory that is disabled is not remapped.

System BIOS Area (F0000–FFFFFh)

This area is a single 64-Kbyte segment that can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to PCI. By manipulating the read/write attributes, the SoC can “shadow” BIOS into main memory. Memory that is disabled is not remapped.

6.1.2. Extended Memory Region

This memory region covers 10_0000h (1 Mbyte) to FFFF_FFFFh (4 Gbytes minus 1) address range and is divided into the following regions:

- DRAM memory from 1 Mbyte to a top of memory
- PCI Memory space from the top of memory to 4 Gbytes
- High BIOS area from 4 Gbytes to 4 Gbytes minus 16 Mbytes

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 Mbyte to the top of main memory is mapped to the main memory address range controlled by the SoC. All accesses to addresses within this range are forwarded to the main memory.

PCI Memory Address Range (Top of Main Memory to 4 Gbytes)

The address range from the top of main DRAM to 4 Gbytes is normally mapped to PCI. The PMC forwards all accesses within this address range to PCI.

High BIOS Area (FF00_0000–FFFF_FFFFh)

The top 16 Mbytes of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is aliased to 16 Mbytes minus 256 Kbytes range. The actual address space required for the BIOS is less than 2 Mbytes. However, the minimum CPU MTRR range for this region is 2 Mbytes. Thus, the full 2 Mbytes must be considered.

6.2. Memory Shadowing

Any block of memory that can be designated as read only or write only can be “shadowed” into PMC DRAM memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read only during the copy process while DRAM at the same time is designated write only. After copying, the DRAM is designated read only so that ROM is shadowed. CPU bus transactions are routed accordingly. The PMC does not respond to transactions originating from PCI or ISA masters and targeted at shadowed memory blocks.

6.3. I/O Address Space

The SoC positively decodes accesses to all internal registers, including PCI configuration registers (CF8h and CFCh), PC/AT Compatible I/O registers (8237, 8254 & 8259), and all relocatable I/O space registers (UART).

