HIKSEMI

HSEMTCY2D2B64GG

Industry eMMC5.1

Table of Content

1 Introduction 2
1.1 General Description 2
1.2 Features Overview 2
2 Block Diagram 3
3 Physical Specifications 4
3.1 153 Ball Pin Configuration 4
3.2 Pins and Signal Description 4
3.3 Package Dimension 5
4 Bus Circuitry Diagram 7
5 Product Specifications 7
5.1 Performance 7
5.2 User Density 7
5.3 Pre-Burned Capacity 8
5.4 Supply Voltage 9
5.5 Power Consumption 9
6 e•MMC Interface 9
6.1 e•MMC Power Up 9
6.2 e•MMC H/W Reset 10
6.3 e•MMC Power Cycling 10
6.4 e•MMC Timing Parameter 11
7 Device Register 12
7.1 OCR Register 12
7.2 CID Register 12
7.3 CSD Register 12
7.4 Extended CSD Register 14

1 Introduction

1.1 General Description

HIKSEMI e•MMC is a hybrid device combining an embedded thin flash controller and standard TLC NAND flash memory, with an industry standard e•MMC 5.1 interface.

Table 1: Product Information

Capacity	Part Number	NAND Flash Type	Package Size	Package Type
64GB	HSEMTCY2D2B64GG	3D TLC 256Gb x2	11.5x13x1.0 (mm)	153 FBGA

1.2 Features Overview

JEDEC/MMC standard version 5.1-compliant

- Backward compatible to e•MMC v4.5 to v5.1

Data bus width : 1bit (Default), 4bit, 8bit

Operating voltage range

- VCC (NAND): 2.7–3.6V
- VCCQ (Controller): 1.7–1.95V/ 2.7–3.6V

Temperature range

- Operating temperature range: –40℃ to +85℃
- Storage temperature range: –40℃ to +85℃

MMC –Specific Feature

- HS400/Clock frequencies 0~200MHz
- Support Single Data Rate(SDR) and Dual Data Rate(DDR)
- Original Boot and Alternative Boot modes
- Hardware reset signal
- Data Removal commands: Erase, Trim, Sanitize and Discard
- Multiple Partitioning
- Signed access to a Replay Protected Memory Block
- Replay Protected Memory Block(RPMB)
- Lock/Unlock and Write Protection
- Data protection mechanisms: Password/Permanent/Power-on/Temporary
- Support Sleep/Awake
- Power off notification

2 Block Diagram

The e•MMC can be operated in 1, 4, or 8-bit mode. NAND flash memory is managed by a controller inside, which manages ECC, wear leveling and bad block management. e•MMC provides easy integration with the host process that all flash management hassles are invisible to the host.

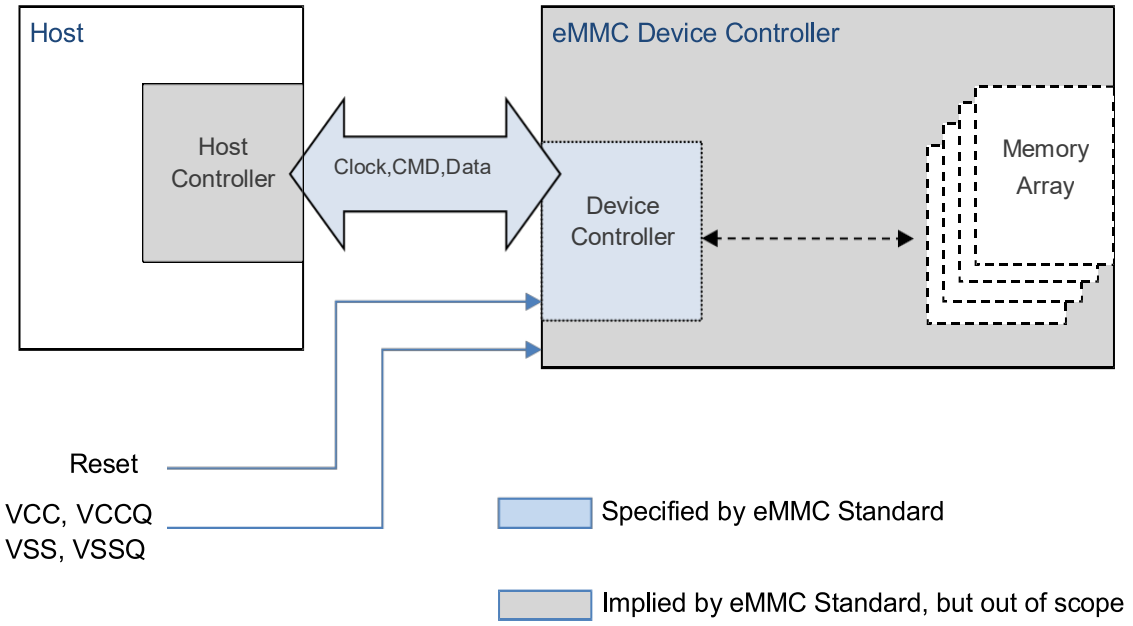


Figure 1 HIKSEMI eMMC I/F Block Diagram

3 Physical Specifications

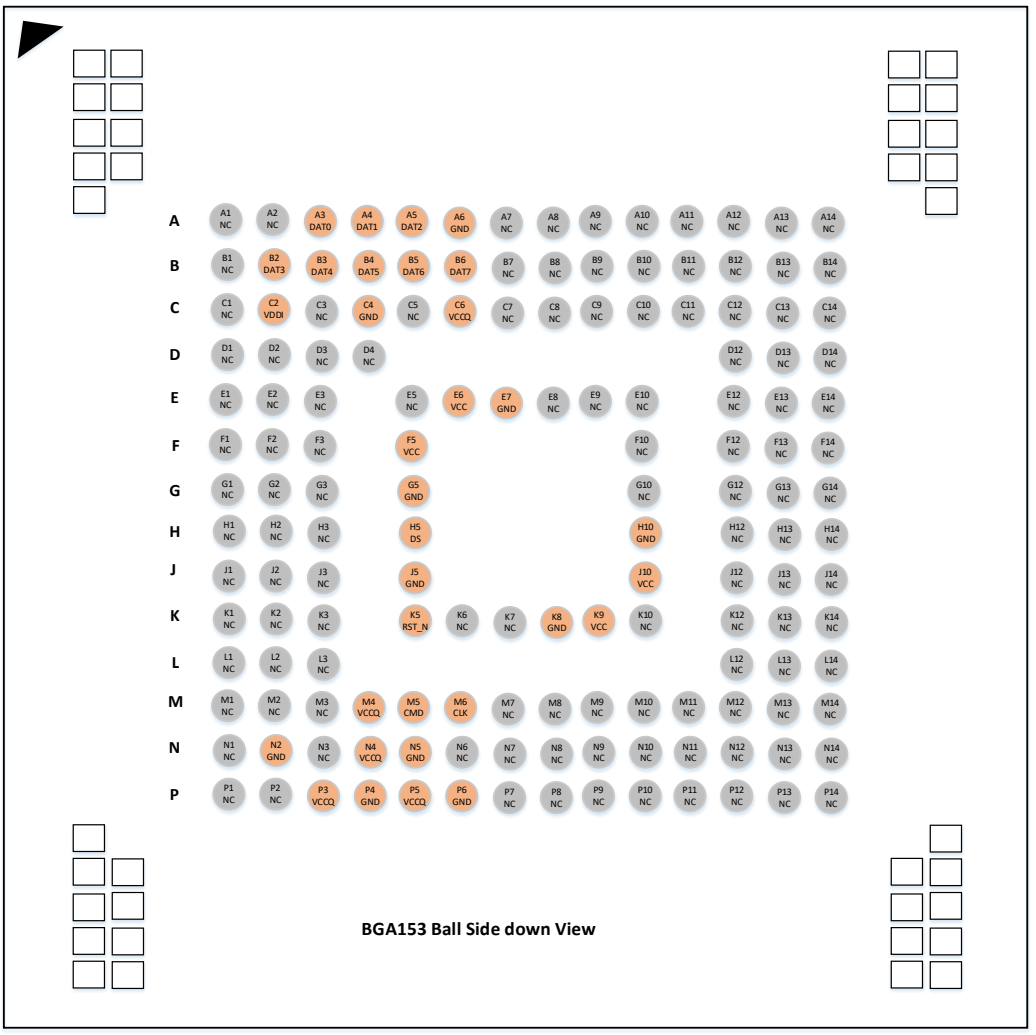


Figure 2 153 Ball Pin Configuration

Table 2: Ball Side down View

Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A3	DAT0	C2	VDDi	H10	GND	N4	VCCQ
A4	DAT1	C4	GND	J10	VCC	N5	GND
A5	DAT2	C6	VCCQ	K5	RST_n	P3	VCCQ
A6	GND	E6	VCC	K8	GND	P4	GND
B2	DAT3	E7	GND	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	GND
B4	DAT5	G5	GND	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	J5	GND	N2	GND		

3.2 Pins and Signal Description

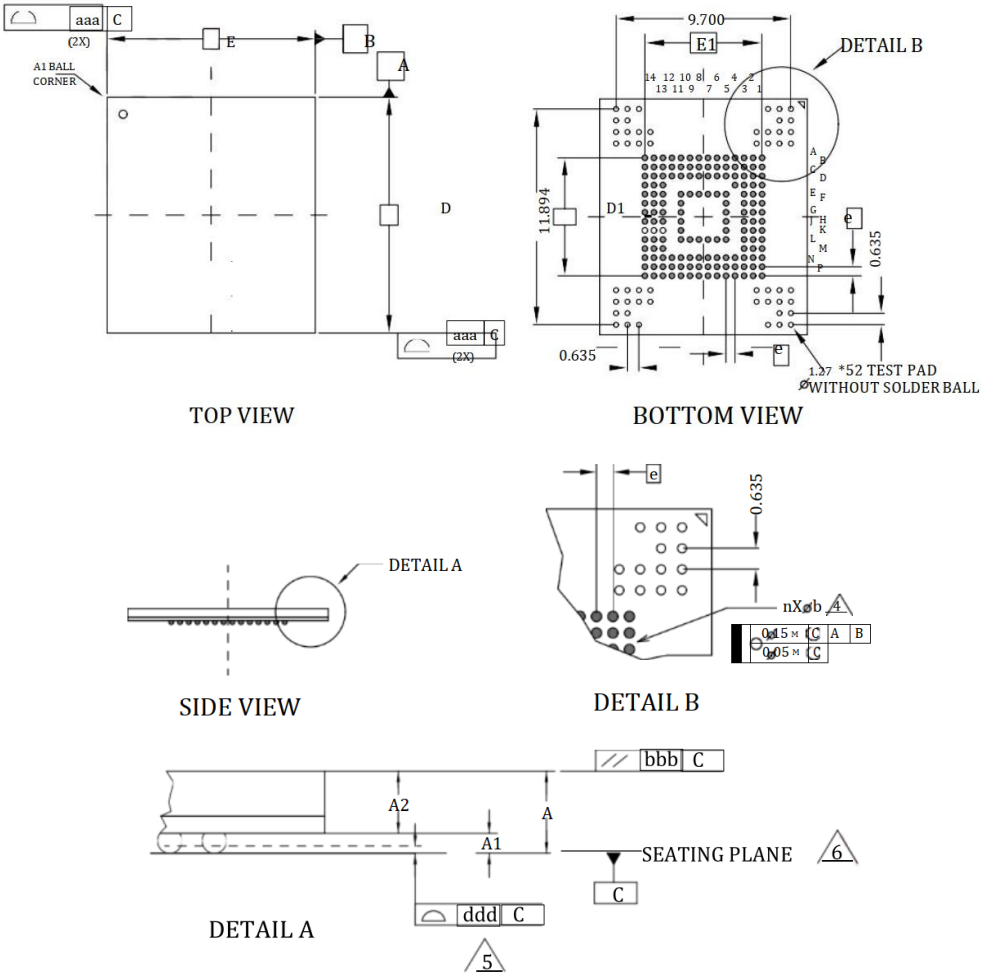
Table 3: Pins and Signal Description

Symbol	Type	Ball Function
CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines.

CMD	Input	Command: A bidirectional channel used for device initialization and command transfer. Command has two operating mode : Open-drain for initialization. Push-pull for fast command transfer.
DAT0	I/O	Data I/O0: Bidirectional channel used for data transfer.
DAT1	I/O	Data I/O1: Bidirectional channel used for data transfer.
DAT2	I/O	Data I/O2: Bidirectional channel used for data transfer.
DAT3	I/O	Data I/O3: Bidirectional channel used for data transfer.
DAT4	I/O	Data I/O4: Bidirectional channel used for data transfer.
DAT5	I/O	Data I/O5: Bidirectional channel used for data transfer.
DAT6	I/O	Data I/O6: Bidirectional channel used for data transfer.
DAT7	I/O	Data I/O7: Bidirectional channel used for data transfer.
RST_n	Input	Reset signal pin
DS	Output	DS: data strobe
VCC	Supply	VCC: Flash memory I/F and Flash memory power supply.
VCCQ	Supply	VCCQ: Memory controller core and MMC interface I/O power supply.
VSS	Supply	VSS: Flash memory I/F and Flash memory ground connection.
VSSQ	Supply	VSSQ: Memory controller core and MMC I/F ground connection
VDDi		VDDi : Connect 1uF capacitor from VDDi to ground.

3.3 Package Dimension

HIKSEMI eMMC is a 153-pin, thin fine-pitched ball grid array (BGA) and its size is 11.5mm×13.0mm×1.0mm.max.



DIMENSIONAL REFERENCES				
REF.	MIN.	NOM.	MAX.	
A	-	-	1.00	
A1	0.17	0.22	0.27	
A2	0.69 REF.			
D	13.00 BSC.			
D1	6.50 BSC.			
E	11.50 BSC.			
E1	6.50 BSC.			
b	0.26	0.31	0.36	4
aaa	0.10			
bbb	0.10			
ddd	0.08			
e	0.50 BSC.			
MD/ME	14 / 14			
n	153			
REF.: JEDEC MO-276H				8

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'M' REPRESENTS THE BASIC SOLDER BALL MATRIX SIZE FOR 0.50 PITCH. AND SYMBOL 'n' IS THE NUMBER OF BALLS AFTER DEPOPULATING.

4. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DAIUM C.

5. DIMENSION 'ddd' IS MEASURED PARALLEL TO PRIMARY DATUM C.

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THESPHERICAL CROWNS OF THE SOLDER BALLS.

7. PACKAGE SURFACE SHALL BE MATTE FINISH CHARMILLES 24 TO 27.

8. EXCEPTION IS "b" DIMENSIONS.

9. TOLERANCE OF OVERALL PACKAGE THICKNESS IS DEFINED BY RSS.

Unit: mm

Figure 3 Package Dimension Diagram

4 Bus Circuitry Diagram

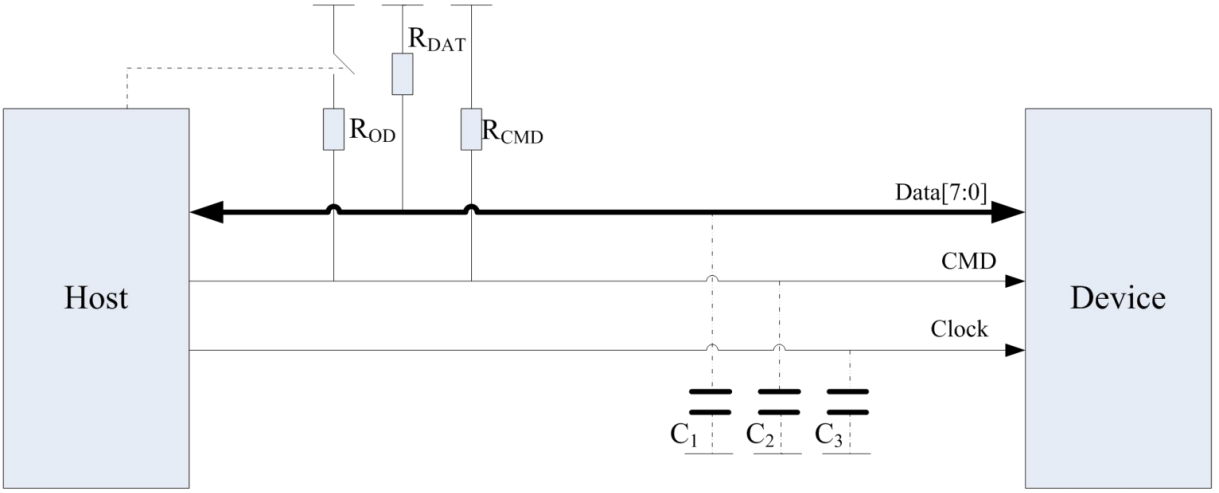


Figure 4 Bus Circuitry Diagram

5 Product Specifications

5.1 Performance

Table 4: Sequential Performance

Capacity	Part Number	Work Mode	Sequential Read.max(MB/s)	Sequential Write .max(MB/s)
64GB	HSEMTCY2D2B64GG	HS400	UP to 290	UP to 200

Test Condition: GL3227 Card Reader, USB3.0, FAT32 File System, OS less, Clean State.

Table 5: Random Performance

Capacity	Part Number	Work Mode	R.R.(IOPS)	R.W.(IOPS)
64GB	HSEMTCY2D2B64GG	HS400	UP to 3500	UP to 3200

Test Condition: GL3227 Card Reader, USB3.0, FAT32 File System, OS less, Clean State.

5.2 User Density

The default area of the memory device consists of a User Data Area to store data, two possible boot area partitions for booting and the Replay Protected Memory Block Area Partition to manage data in an authenticated and replay protected manner. The memory configuration initially consists(before any partitioning operation) of the User Data Area and RPMB Area Partitions and Boot Area Partitions.

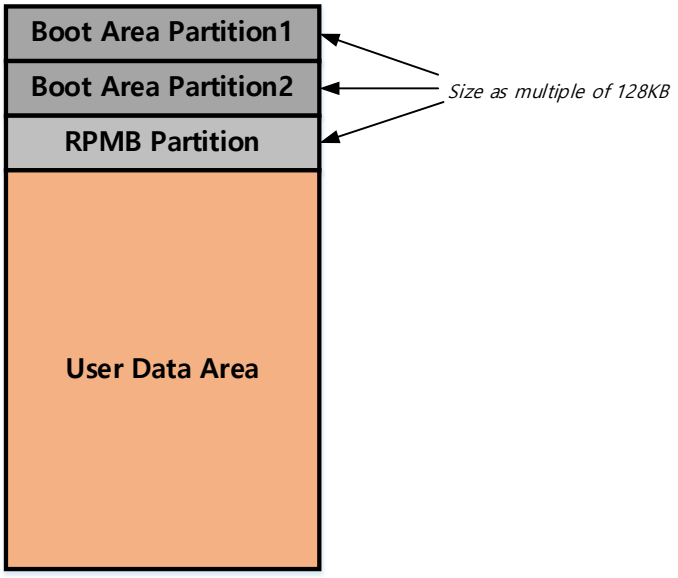


Figure 5 Space Allocation in device

Table 6: Boot Partition & RPMB

Capacity	Part Number	Boot Partition1	Boot Partition2
64GB	HSEMTCY2D2B64GG	4,096KB	4,096KB

Table 7: User Density Size

Capacity	Part Number	User Area Capacity	SEC_COUNT in Extended CSD
64GB	HSEMTCY2D2B64GG	59640 MB	0x747C000

Table 8: Maximum Enhanced Partition Size

Capacity	Part Number	Max. Enhanced Partition Size	MAX_ENH_SIZE_MULT	HC_WP_GRP_SIZE	HC_ERASE_GRP_SIZE
64GB	HSEMTCY2D2B64GG	19824MB	0x4D7	0x20	0x1

Max Enhanced Area = MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512Kbytes

5.3 Pre-Burned Capacity

e•MMC provides a certain Pre-Burned capacity(PBC) in FOB state for customer burn data to e•MMC before the PCBA being SMT. The amount of data written before SMT should less than PBC.

Table 9: Maximum Pre-Burned Capacity

Capacity	**Part Number**	**Pre-Burned Capacity**	**Reflow**
64GB	HSEMTCY2D2B64GG	19.36GB	3 times

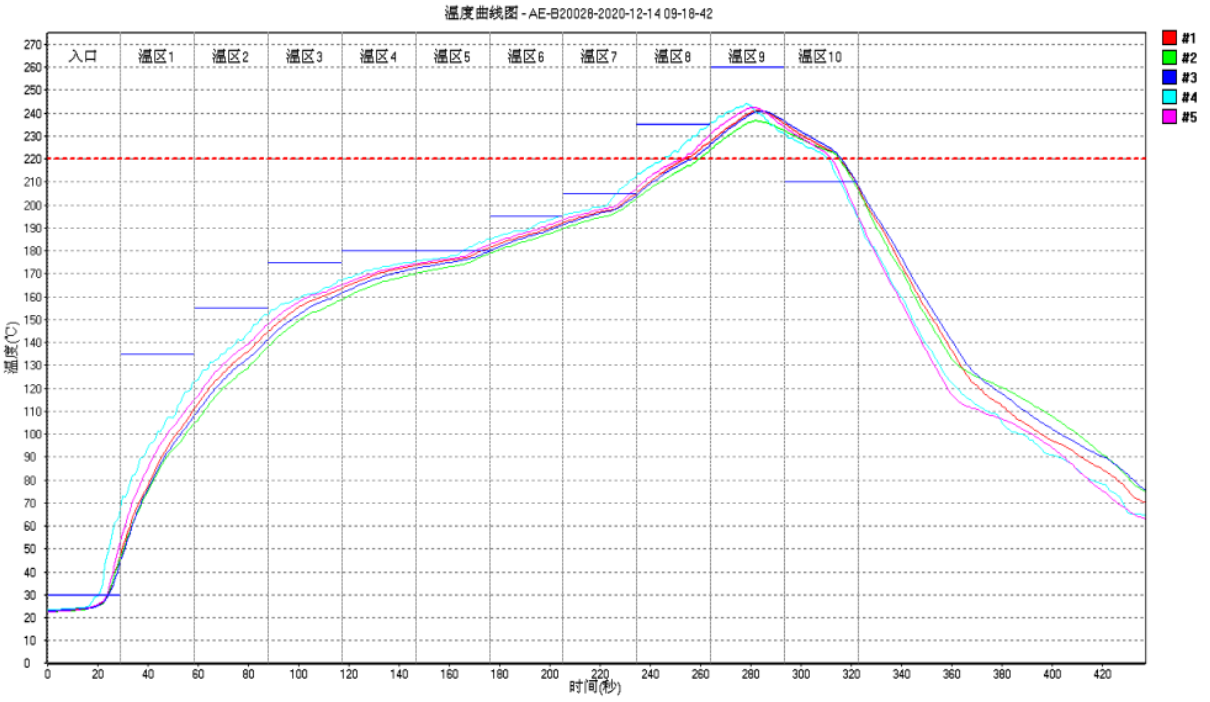


Figure 6 Temperature curve during reflow test

5.4 Supply Voltage

Table 10: Supply Voltage

Parameter	Symbol	Min	Max	Typ	Unit
Supply voltage1 (NAND/Core)	V_{CC}	2.7	3.6	3.3	V
Supply voltage 2 (CTRL/IO)	V_{CCQ}	1.7	1.95	1.8	V
		2.7	3.6	3.3	V

5.5 Power Consumption

Table 11: Operating Current (RMS): Active Power Consumption during operation

Capacity	Operation	Icc (Max)	Iccq (Max)	Unit
64GB	Read	60	120	mA
	Write	45	65	

Note

Max RMS current is the average RMS current consumption over a period of 100ms.
Temperature: 25℃
V_{CC}=3.3V, V_{CCQ}=1.8V
Not 100% tested

Table 12: Standby Power Consumption in auto power saving mode and standby state

Capacity	State	Icc	Iccq	Unit
64GB	Standby	10	75	uA

Note

Power measurement conditions: Bus configuration =x8, No CLK
V_{CC}=3.3V, V_{CCQ}=1.8V
Not 100% teste

Table 13: Sleep Power Consumption in Sleep State

Capacity	State	Icc	Iccq	Unit
64GB	Sleep	0	75	uA

Note

Power measurement conditions: Bus configuration = x8, No CLK
Enter sleep state by CMD5, V_{CC} power is switched off, V_{CCQ}=3.3V
Not 100% tested

6 e•MMC Interface

6.1 e•MMC Power Up

An eMMC bus power-up is handled locally in each device and in the bus master. Figure 3 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B51 for specific instructions regarding the power-up sequence.

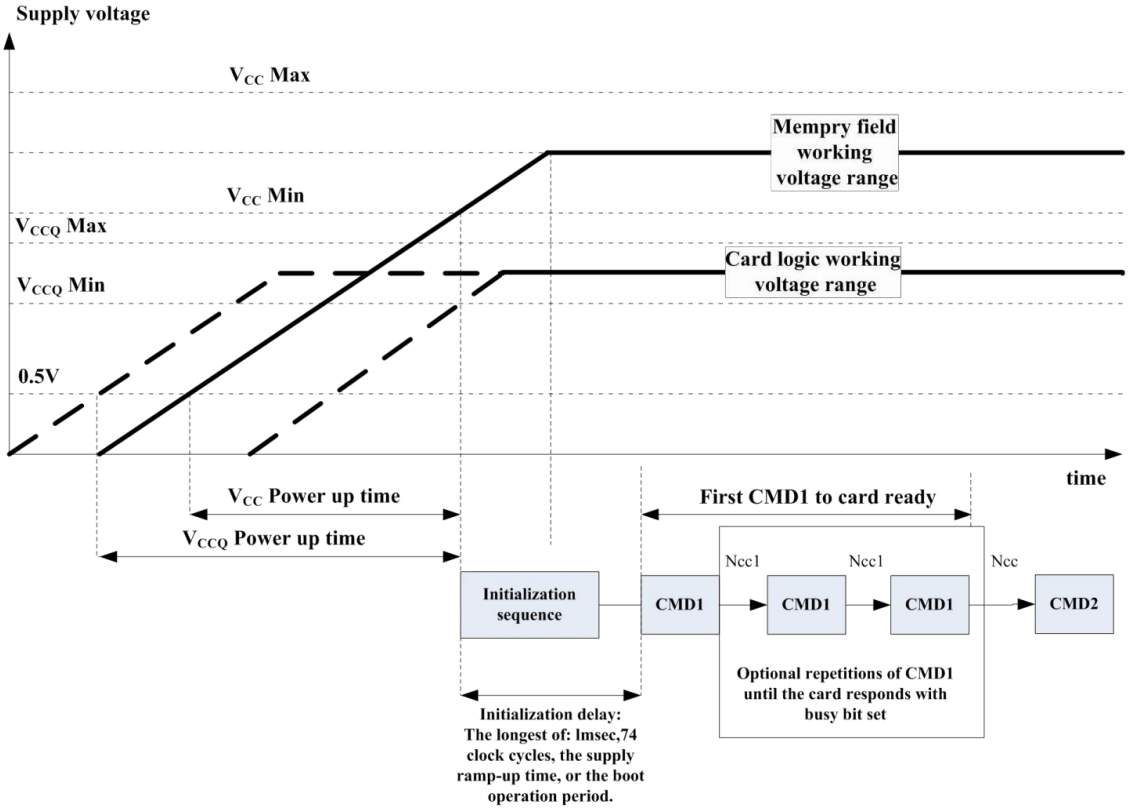


Figure 7 e•MMC Power-up Diagram

Power-up parameter

After power up, the e•MMC enters the pre-idle state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

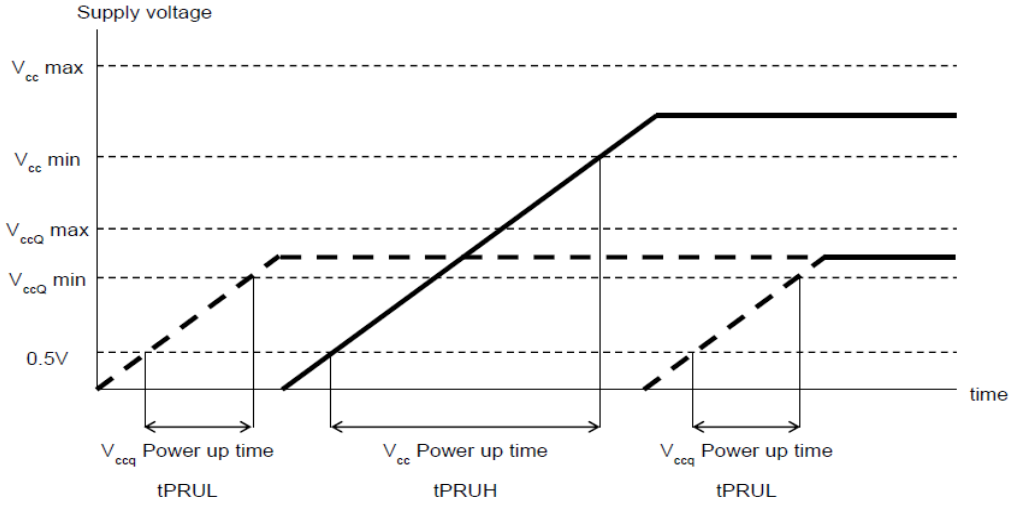


Figure 8 e•MMC Power-up Parameter Diagram

Table 14: Power-up parameter

Parameter	Symbol	Min	Max	Remark
Supply power-up for 3.3V	tPRUH	5 µs	35 ms	--
Supply power-up for 1.8V	tPRUL	5 µs	25 ms	--

6.2 e•MMC H/W Reset

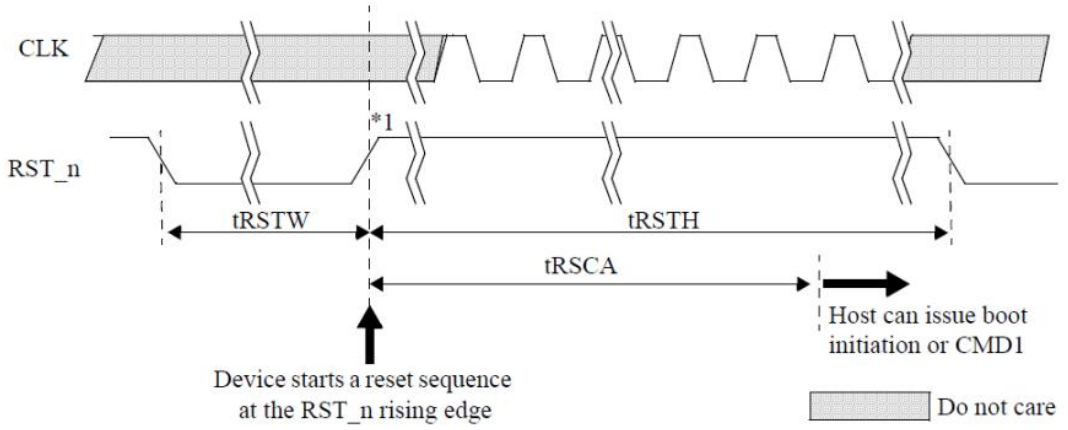


Figure 9 e•MMC H/W Reset Diagram

Table 15: H/W Reset Timing Parameters

Symbol	Comment	Min	Max	Unit
t_{RSTW}	RST_n pulse width	1	--	µs
t_{RSCA}	RST_n to Command time	200 [1]	--	µs
t_{RSTH}	RST_n high period (interval time)	1	--	µs

Note

74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA.

6.3 e•MMC Power Cycling

The master can execute any sequence of VCC and VCCQ power-up/power-down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down VCC to reduce power consumption. It is necessary for the slave to be ramped up to VCC before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B51.

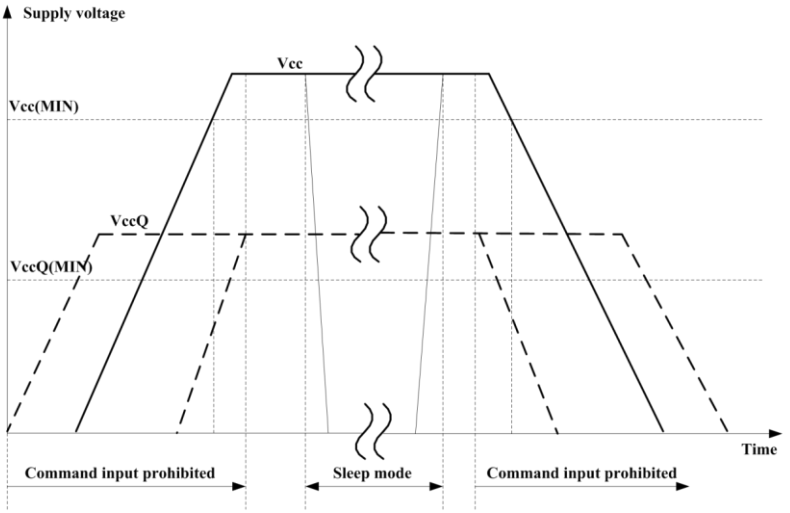


Figure 10 e•MMC Power Cycle Diagram

6.4 e•MMC Timing Parameter

Table 16: Timing Parameter

Timing Parameter		Max. Value	Unit
Initialization Time (t_{INIT})	Normal	1	s
	After partition setting	1	s
Read Timeout		200	ms
Write Timeout		200	ms
Erase Timeout		300	ms
Force Erase Timeout		3	min
Secure Erase Timeout		0.3	s
Secure Trim Timeout		5.1	s
Trim Timeout		600	ms
Partition Switching Timeout (after Init)		500	ms
Power Off Notification (Short) Timeout		500	ms
Power Off Notification (Long) Timeout		600	ms

Note

Normal Initialization Time without partition setting
Initialization Time after partition setting, refer to INI_TIMEOUT_AP in EXT_CSD register
Be advised Timeout Values specified in Table above are for testing purposes under internal test pattern only and actual timeout situations may vary
EXCEPTION_EVENT may occur and the actual timeout values may vary due to user environment.

7 Device Register

7.1 OCR Register

The 32-bit operation conditions register (OCR) stores the V_{DD} voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 17: OCR Register Value

OCR bit	VDD voltage window	Value	Width
[31]	eMMC power up status bit (busy)1=READY*		
[30:29]	Access mode	10b (sector mode)	2
[28:24]	Reserved	0 0000b	5
[23:15]	2.7–3.6V	1 1111 1111b	9
[28:24]	Reserved	000 0000b	
[14:8]	2.0–2.6V	000 0000b	7
[7]	1.70–1.95V	1b	1
[6:0]	Reserved	000 0000b	7

Note

* This bit is set to LOW if the e•MMC has not finished the power up routine. The supported voltage range is coded as shown in table.

7.2 CID Register

The Device IDentification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (e•MMC protocol). Every individual flash or I/O Device shall have a unique identification number. Every type of e•MMC Device shall have a unique identification number. The structure of the CID register is defined in this section.

Table 18: CID Register Value

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x2C
Reserved	-	6	[119:114]	-
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x0E
Product name	PNM	48	[103:56]	0x54 0x43 0x59 0x32 0x44 0x32（TCY2D2）
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN	32	[47:16]	Serial number
Manufacturing date	MDT	8	[15:8]	Manufacturing date
CRC7 checksum	CRC	7	[7:1]	--
Not used; always 1	---	1	0	--

7.3 CSD Register

The Card-Specific Data register provides information on how to access the e•MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:

R: Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P:Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table 19: CSD Register Value

Name	Field	Width	Cell Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:104]	0x2F
Data read access-time 2	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x2A
Card command classes	CCC	12	R	[95:84]	0xDF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77]	0x00
DSR implemented	DSR_IMP	1	R	[76]	0x00
Reserved	-	2	R	[75:74]	-
Card size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x1F
Write protect group enable	WP_GRP_ENABLE	1	R	[31]	0x01
Manufacturer default	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x01
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21]	0x00
Reserved	-	4	TBD	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
Calculated CRC	CRC	7	R/W/E	[7:1]	--
Not used, always'1'	--	1	—	[0:0]	--

7.4 Extended CSD Register

The Extended CSD register defines the e•MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e•MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e•MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R: Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table 20: Extended CSD Register Value

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Properties Segment					
Reserved	-	6	TBD	[511:506]	-
Extended Security Commands Error	EXT_SECURITY_ERR	1	R	[505]	0x00
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI Features	HPI_FEATURES	1	R	[503]	0x03
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x01
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	0x00
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x00
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01
FFU features	FFU_FEATURES	1	R	[492]	0x01
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	R	[491]	0x17
FFU Argument	FFU_ARG	4	R	[490:487]	0x00
Barrier support	BARRIER_SUPPORT	1	TBD	[486]	0x00
Reserved	Reserved	177	-	[309:485]	-

CMDQ support	CMDQ_SUPPORT	1	R	[308]	0x00
CMDQ depth	CMDQ_DEPTH	1	R	[307]	0x00
Reserved	Reserved	1	-	[306]	-
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_ CORRECTLY_PROGRAMMED	4	R	[305:302]	0x0
Vendor proprietary health report	VENDOR_PROPRIETARY_HEAL TH_REPORT	32	R	[301:270]	--
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_ B	1	R	[269]	TLC Block life time estimation
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_ A	1	R	[268]	SLC Block life time estimation
Pre EOL information	PRE_EOL_INFO	1	R	[267]	Pre EOL
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x08
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x08
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x08
Device version	DEVICE_VERSION	2	R	[263:262]	ExtCSD[263]=0x00
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	--
Power class for 200MHz,DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0x00
Cache size	CACHE_SIZE	4	R	[252:249]	0x100
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x32
Power off notification(long)ti meout	POWER_OFF_LONG_TIME	1	R	[247]	0x3C
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_ NUM	4	R	[245:242]	0x00
1st Initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	TBD	[240]	0x00
Power class for 52MHz, DDR at VCC=3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at VCC=1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Power class for 200MHz at VCCQ=1.95V,VCC =3.6V	PWR_CL_200_195	1	R	[237]	0x00
Power class for 200MHz, at VCCQ=1.3V,VCC= 3.6V	PWR_CL_200_130	1	R	[236]	0x00
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00

Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved	-	1	TBD	[233]	-
TRIM Multiplier	TRIM _MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot Information	BOOT_INFO	1	R	[228]	0x07
Reserved	-	1	TBD	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x20
Access size	ACCESS_SIZE	1	R	[225]	0x06
High Capacity Erase unit size	HC_ERASE_GROUP_SIZE	1	R	[224]	0x01
High capacity erase time out	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x20
Sleep current [VCC]	S_C_VCC	1	R	[220]	0x07
Sleep current [VCCQ]	S_C_VCCQ	1	R	[219]	0x07
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x17
Sleep/Awake time out	S_A_TIMEOUT	1	R	[217]	0x17
Sleep Notification Timout1	SLEEP_NOTIFICATION_TIME	1	R	[216]	0x11
Sector count	SEC_COUNT	4	R	[215:212]	0x747C000
Secure Write Protect Information	SECYRE_WP_INFO	1	R	[211]	0x00
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00

Reserved	-	1	-	[204]	-
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	0x00
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	0x00
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	0x00
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x05
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x19
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x0F
Card Type	CARD_TYPE	1	R	[196]	0x57
Reserved	-	1	-	[195]	-
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved	-	1	-	[193]	-
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x08
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved		1	TBD	[190]	-
Command set revision	CMD_SET_REV		R	[189]	0x00
Reserved		1	TBD	[188]	-
Power class	POWER_CLASS		R/W/E_P	[187]	0x00
Reserved		1	TBD	[186]	-
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x03
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved		1	TBD	[182]	-
Erased memory range	ERASE_MEM_CONT	1	R	[181]	0x00
Reserved		1	TBD	[180]	-
Partition Configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00
Boot Config protection	BOOT_CONFIG_PROT	1	R/W &R/W/C_P	[178]	0x00
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00
Reserved		1	TBD	[176]	0x00
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0x00
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00
Boot area write protect register	BOOT_WP	1	R/W &R/W/C_P	[173]	0x00
Reserved		1	TBD	[172]	-
User area write protect register	USER_WP	1	R/W,R/W/C_P &R/W/E_P	[171]	0x00

Reserved		1	TBD	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x00
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x14
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x01
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x4D7
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved		1	TBD	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x01
Reserved		2	TBD	[129:128]	-
Vendor Specific Fields	NATIVE_SECTOR_SIZE	1	<vendor specific>	[127:64]	0x00
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0x00
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0x00
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00

Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00
Exception events control	EXCEPTION_EVENTS _CTRL	2	R/W/E_P	[57:56]	0x001E
Exception events status	EXCEPTION_EVENTS _STATUS	2	R	[55:54]	0x00
Extended Partitions Attribute	EXT_PARTITIONS_AT TRIBUTE	2	R/W	[53:52]	0x00
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00
Packed command status	PACKED_COMMAND _STATUS	1	R	[36]	0x00
Packed command failure index	PACKED_FAILURE_IN DEX	1	R	[35]	0x00
Power Off Notification	POWER_OFF_NOTIFI CATION	1	R/W/E_P	[34]	0x01
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x01
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00
Mode operation codes	MODE_OPERATION_ CODES	1	W/E_P	[29]	0x00
Reserved		2	TBD	[28:27]	-
FFU status	FFU_STATUS	1	R	[26]	0x00
Pre loading data size	PRE_LOADING_DATA _SIZE	4	R/W/E_P	[25:22]	0x00
Max pre loading data size	MAX_PRE_LOADING _DATA_SIZE	4	R	[21:18]	0x26B8000
Product state awareness enablement	PRODUCT_STATE_A WARENESS_ENABLE MENT	1	R/W/E & R	[17]	0x03
Secure Removal Type	SECURE_REMOVAL_ TYPE	1	R/W & R	[16]	0x09
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00
Reserved		15	TBD	[14:0]	-

Note

Reserved bits should be read as “0”.

Revision History

Version	Description	Date
1.0	Jul.6th,2022	Preliminary
1.1	Dec.12th,2022	Rev1.1

Data subject to change without notice.

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